Neo900 Hackerbus
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The Hackerbus is an interface that allows user-provided circuits to connect directly to power rails and various signals in the Neo900.

Warning: Hackerbus gives access to signals that can upset the operation of the Neo900 and incorrect use may cause permanent damage inside and outside the device. Use with caution !

Characteristics beyond what is specified in this document should be obtained by examining the schematics and the data sheets of the respective components.

*Concept and design requirements.
†Specification details and illustrations.

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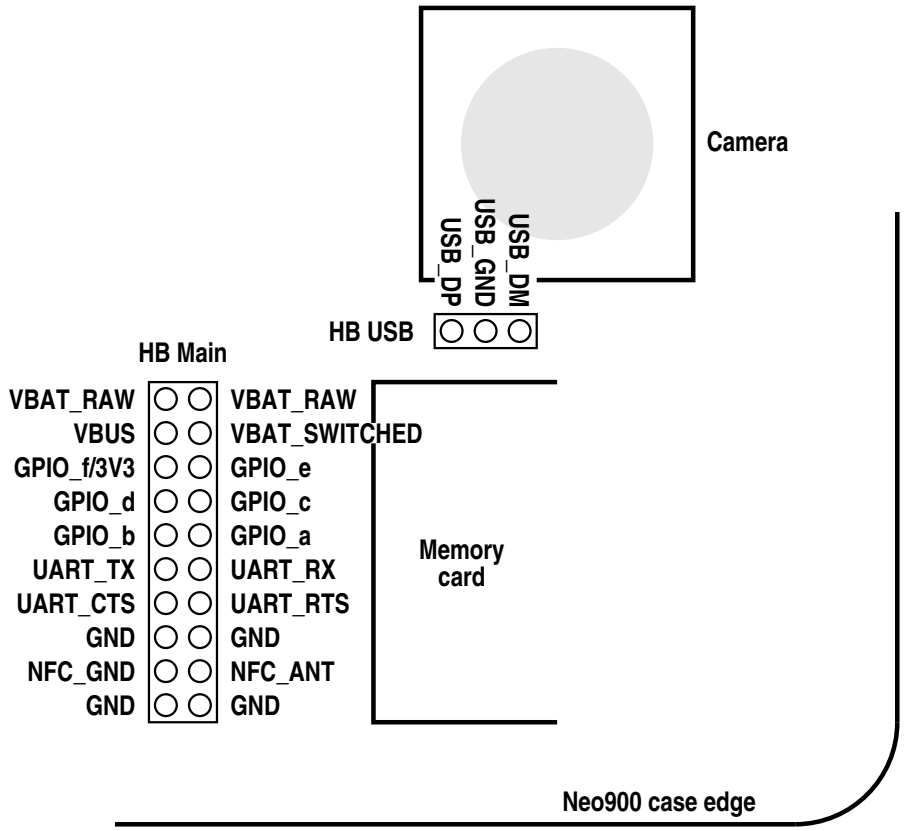
1 Pin assignment

Hackerbus uses two connectors, one for power and various signals and one for USB data, which are arranged around the memory card on the Break-Out-Board (BOB).

The following drawing gives a rough overview of connector locations and shows the pin assignment:



The following table describes the functions of the pins on the Hackerbus main connector:

Hackerbus pin	**Description**
VBAT_RAW	Direct connection to the battery (charging allowed)
VBAT_SWITCHED	Like VBAT_RAW but switched off when system is powered down **Reverse-feed not allowed !**
VBUS	USB bus voltage (reverse-feed allowed)
GND	System ground and return for power and all signals but NFC, USB, and audio
UART_TX	UART3, Transmit data (output from CPU)
UART_RX	UART3, Receive data (input to CPU)
UART_CTS	UART3, Clear To Send (input to CPU)
UART_RTS	UART3, Ready To Send (output from CPU)
GPIO_a	TBD
GPIO_b	TBD
GPIO_c	TBD
GPIO_d	TBD
GPIO_e	TBD
GPIO_f/3V3	TBD / 3.3 V rail
NFC_ANT	NFC antenna, positive
NFC_GND	NFC antenna, ground or negative **Do not connect to any other GND !**

Note that the UART signals may also be used as general IOs and that their role further depends on the configuration of the infrared (IR) subsystem [1].

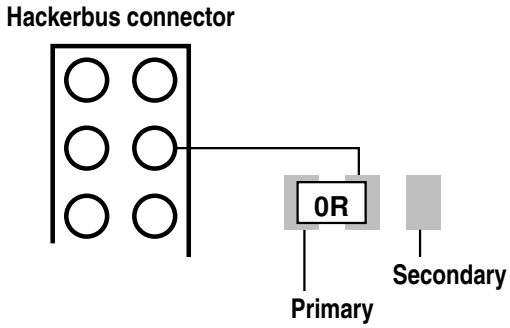
TO DO: The exact function of UART_RX will depend on the implementation of IR RX, which will be decided at a later time.

The Hackerbus USB connector duplicates signals from the Neo900 Micro USB connector:

Hackerbus pin	**Description**
USB_DP	USB differential data, positive
USB_DN	USB differential data, negative
USB_GND	USB signal ground

2 Alternate pin assignments

Some pins have an alternate assignment that can be selected by moving a jumper on the Neo900 PCB. The jumper consists of three pads and a 0 Ω resistor that is soldered in the position that selects the primary function, as shown below:



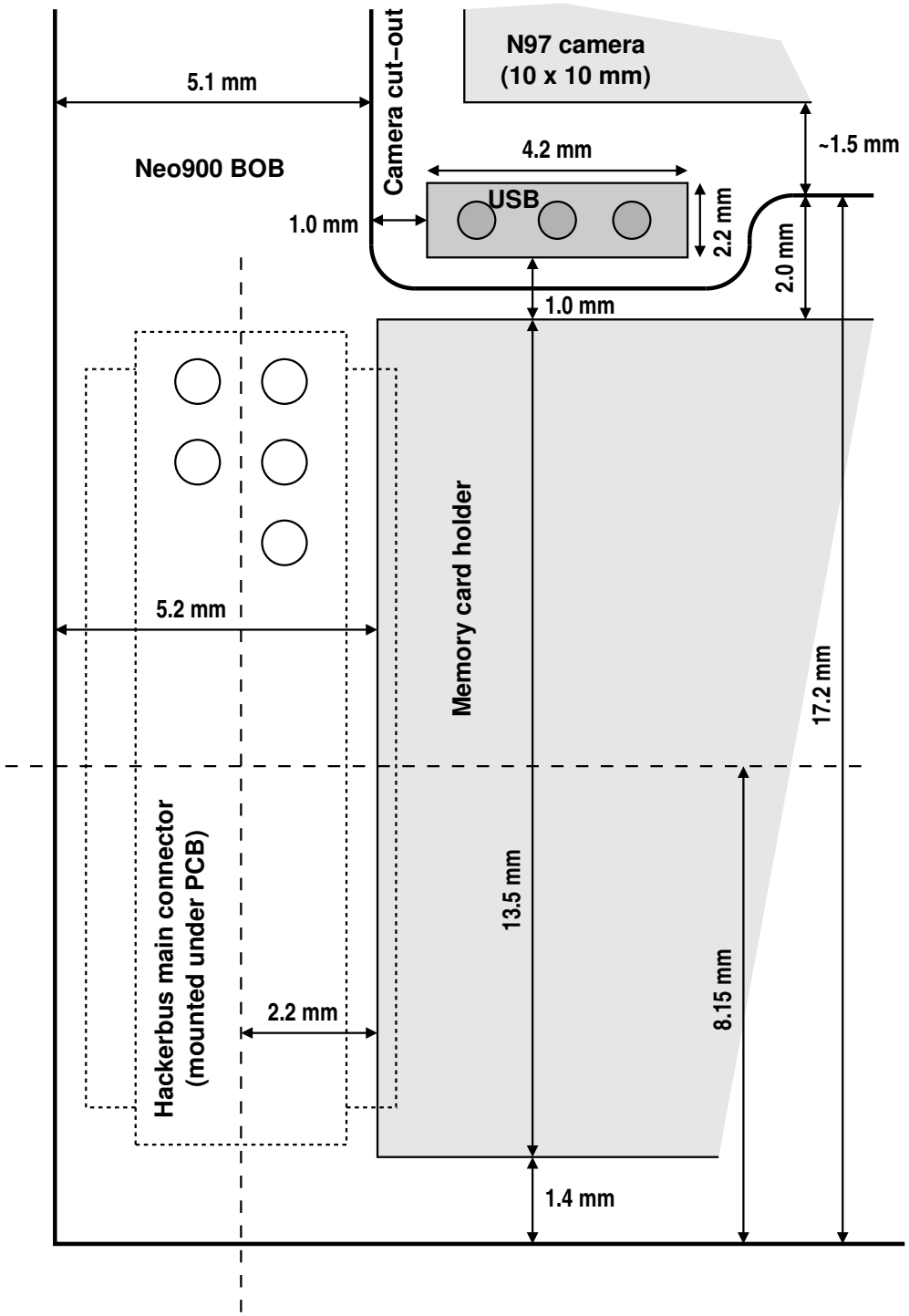
The user can unsolder the resistor and either re-solder it such that it connects to the secondary function, or use jumper wires for any other type of connection.

Jumper	Primary	Secondary
Rxxx	TBD	I2C #3 SDA
Rxxx	TBD	I2C #3 SCL
Rxxx	TBD	Audio out, left
Rxxx	TBD	Audio out, right
Rxxx	TBD	Audio ground
Rxxx	TBD	USB ID

Please note that the secondary functions have ESD protection but only the two I2C signals have level shifters.

3 Physical placement

The following drawing illustrates the precise placement of components on the Break-Out-Board (BOB):



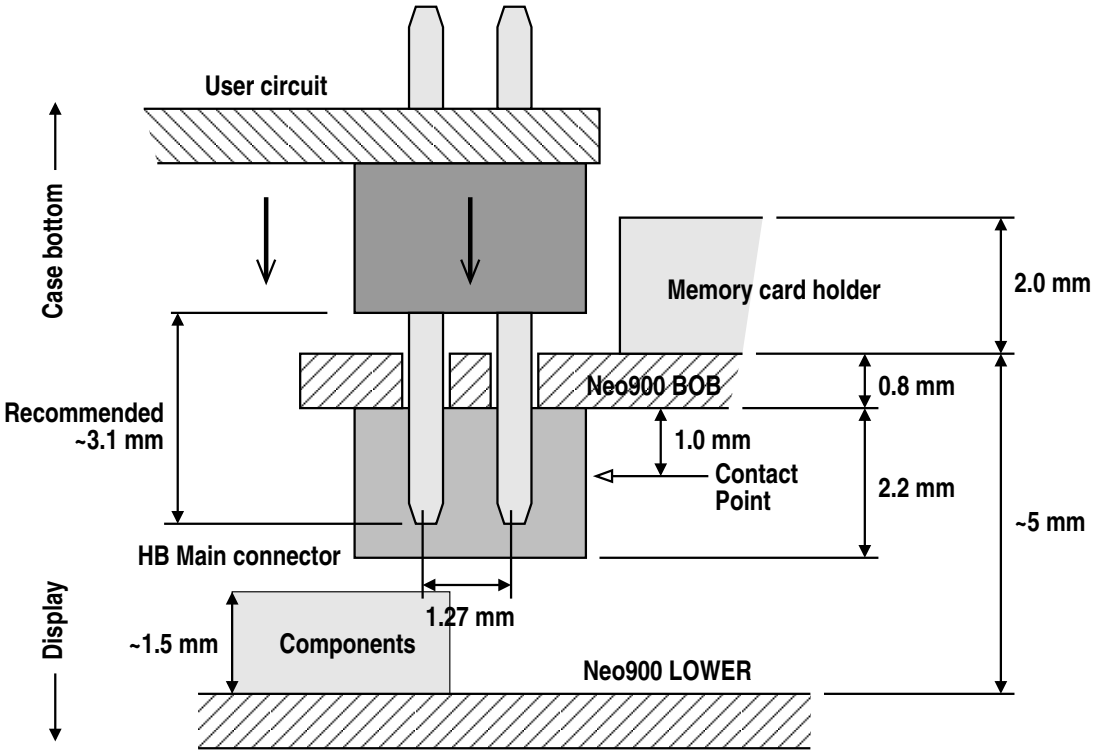
The main connector is soldered to the bottom of the BOB and the header pins pass through holes in the PCB, entering the receptacle from the bottom. The USB connector is soldered to the LOWER board of Neo900 and the whole connector pokes through an opening in the BOB.

Please note that the Hackerbus connectors are covered by plastic structures in the N900 case and are therefore only accessible when the case is removed or if the respective plastic structures have been cut.

3.1 Hackerbus main connector

On the Neo900 side, the principal connector for Hackerbus is a Harwin M50-3150842 [2] female connector with 20 contacts organized in a 10×2 array. The connector has a 1.27 mm pitch and is mounted underneath the Neo900 break-out board (BOB).

The vertical stacking of the main connector is illustrated in the following diagram:[1]



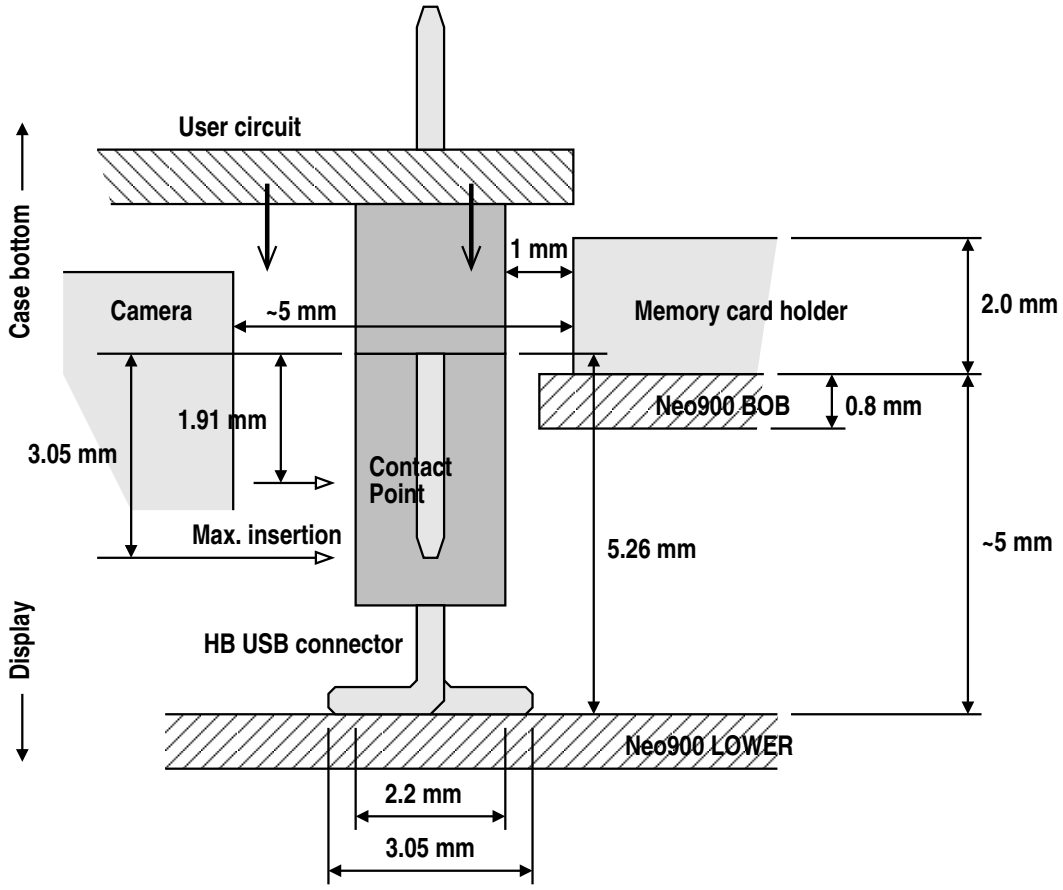
The male header shown as an example in the drawing has the dimensions of the FCI 20021111-00020T4LF through-hole connector,[2] with a contact length of 3.05 mm.

[1] The drawing is approximately to scale but dimensions drawn can be off by up to 0.15 mm in real-world coordinates.
[2] `http://portal.fciconnect.com/Comergent/fci/drawing/20021111.pdf`

3.2 Hackerbus USB connector

On the Neo900 side, the USB connector for Hackerbus is a Mill-Max 851-43-003-30-001000 [3] female connector with one row of 3 contacts.[3] The connector has a 1.27 mm pitch, is mounted on the Neo900 LOWER board, and is accessed through a cut-out in the BOB.

The vertical stacking of the main connector is illustrated in the following diagram:



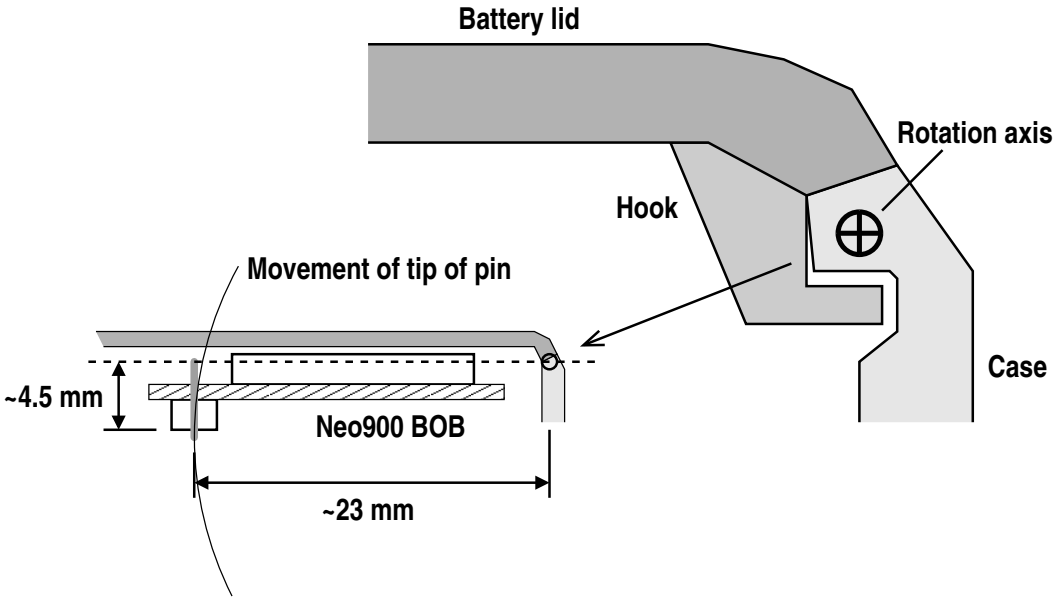
The male header shown as an example in the drawing has the dimensions of the Mill-Max 850-10-050-10-001000 through-hole connector.[4]

3.3 Mechanical coupling with battery cover

If the user circuit connecting to Hackerbus is mechanically coupled with the battery cover, the movement when opening and closing the battery compartment has to be considered. The following drawing shows approximately how the parts involved move:

[3] Availability of the customized 3 pin variant may be limited and it may be more cost-effective to cut pieces from the 50 pin 851-43-050-30-001000.

[4] `https://www.mill-max.com/assets/pdfs/metric/034M.PDF`



The cover has a hook that goes into an opening in the case. When opening or closing the cover it rotates around that hook, which results in anything mechanically connected to the cover to perform the same rotation.

The drawing shows the path along which a header pin plugging into the Hackerbus main connector moves. This rotation may make it difficult to connect extensions whose Hackerbus connector is rigidly coupled with the battery cover. These difficulties would be more pronounced for the Hackerbus USB connector since it is closer to the axis around which the battery cover rotates.

Possible ways to avoid this issue include not coupling the extension with the battery lid, using a flexible coupling, or removing the hook on the cover.

4 Overcurrent protection

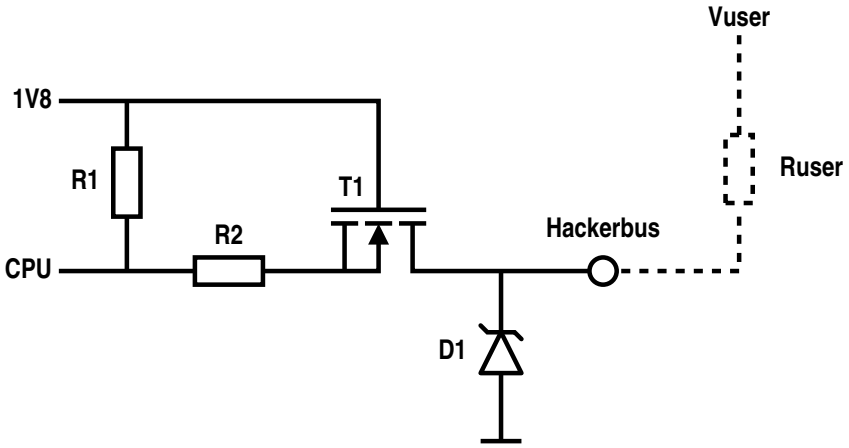
To protect traces and other components from excessive current, VBAT_RAW is equipped with a resettable fuse. Traces and contacts between battery and Hackerbus are designed to be able to permanently conduct at least the trip current of the fuse.

Note that the presence of this fuse does not guarantee that loads exceeding the trip current will not lead to malfunction. Furthermore, the battery is a user-provided item and needs to be evaluated separately by prospective users of VBAT_RAW. The maximum current available on VBAT_RAW depends not only on the fuse but also on the characteristics and condition of the battery.

Peripherals using VBAT_RAW should connect to both VBAT_RAW contacts with traces that each are capable of carrying the full maximum current the application demands.

5 Level shifters

Level shifters are provided to interface with circuits operating in other domains than 1.8 V. The circuit is as follows, for each primary UART and GPIO signal:



The principle of operation is briefly described in [4] and further details can be found in [5]. R1 is usually an internal pull-up resistor in the CPU of 10 kΩ or higher. R2 limits the current when CPU and external circuit drive the Hackerbus signal in a conflicting way. R2 is 100 Ω. D1 protects against ESD and polarity inversion.

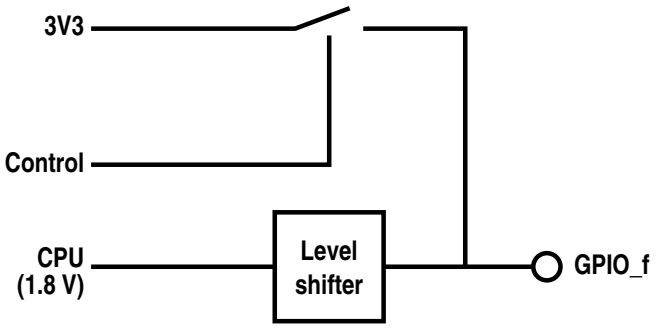
Note that our circuit differs from the NXP design in that Neo900 does not provide a pull-up resistor on the high-voltage side. If the user circuit needs a pull-up, e.g., to drive a logic input, it therefore has to provide one itself. If an external pull-up is to be used, it should be dimensioned such that it does not deliver more than 1.8 mA into the Neo900 if the corresponding Hackerbus signal is driven low (0 V). A value of 10 kΩ or larger is recommended.

Power, NFC, USB, and secondary signals (other than I2C) are not equipped with level shifters.

Further limits and characteristics of this circuit are to be determined by the user.

6 Switchable power rail

The 3.3 V power rail can be switched to the GPIO_f pin under software control. If not operating as power rail, GPIO_f can be used for regular IO. The following drawing illustrates the circuit:



The connection to the CPU is protected by the same circuit as all other IOs available on the Hackerbus. When GPIO_f is configured as power rail, the CPU should set the corresponding GPIO to High-Z without pull-up or -down. The CPU may read the GPIO, but the resulting value is undefined.

TO DO: Determine whether we will have 3.3 V as described here or whether we have a spare LDO that could also provide other voltages.

7 References

[1] Reisenweber, Jörg; Almesberger, Werner. *GTA04b7 Infrared Subsystem*, August 2014. http://neo900.org/stuff/papers/ir.pdf

[2] Harwin. *1.27mm pitch DIL SMT vert low-profile socket assy*, M50-315XX42, March 2013. http://harwin.com/includes/pdfs/M50-315.pdf

[3] Mill-Max Mfg. Corp. *Interconnects – Series 850, 851, 852, 853; 1,27 grid surface mount headers and sockets; single and double row strips*, http://www.mill-max.com/assets/pdfs/metric/037M.PDF

[4] NXP Semiconductors. *Level shifting techniques in I^2C-bus design*, AN10441, Rev. 01, June 2007. http://www.nxp.com/documents/application_note/AN10441.pdf

[5] Schutte, Herman. *Bi-directional level shifter for I^2C-bus and other systems*, AN97055, August 1997, Philips Semiconductors Systems Laboratory Eindhoven. http://www.adafruit.com/datasheets/an97055.pdf