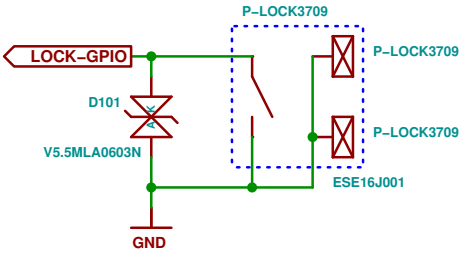
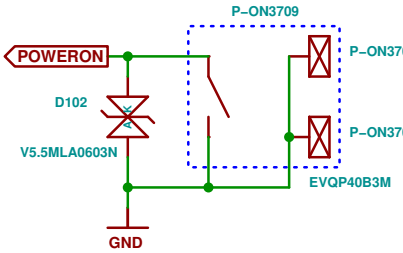
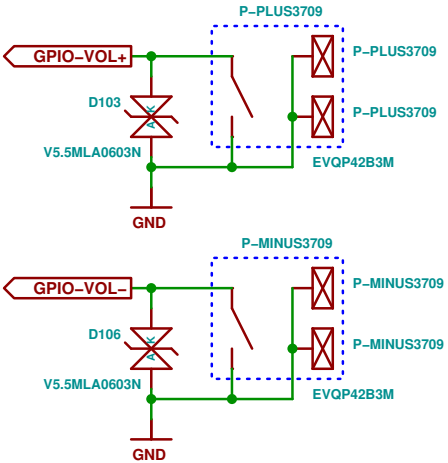
lock switch



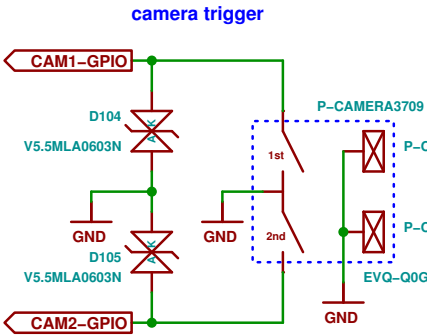
on-off



volume

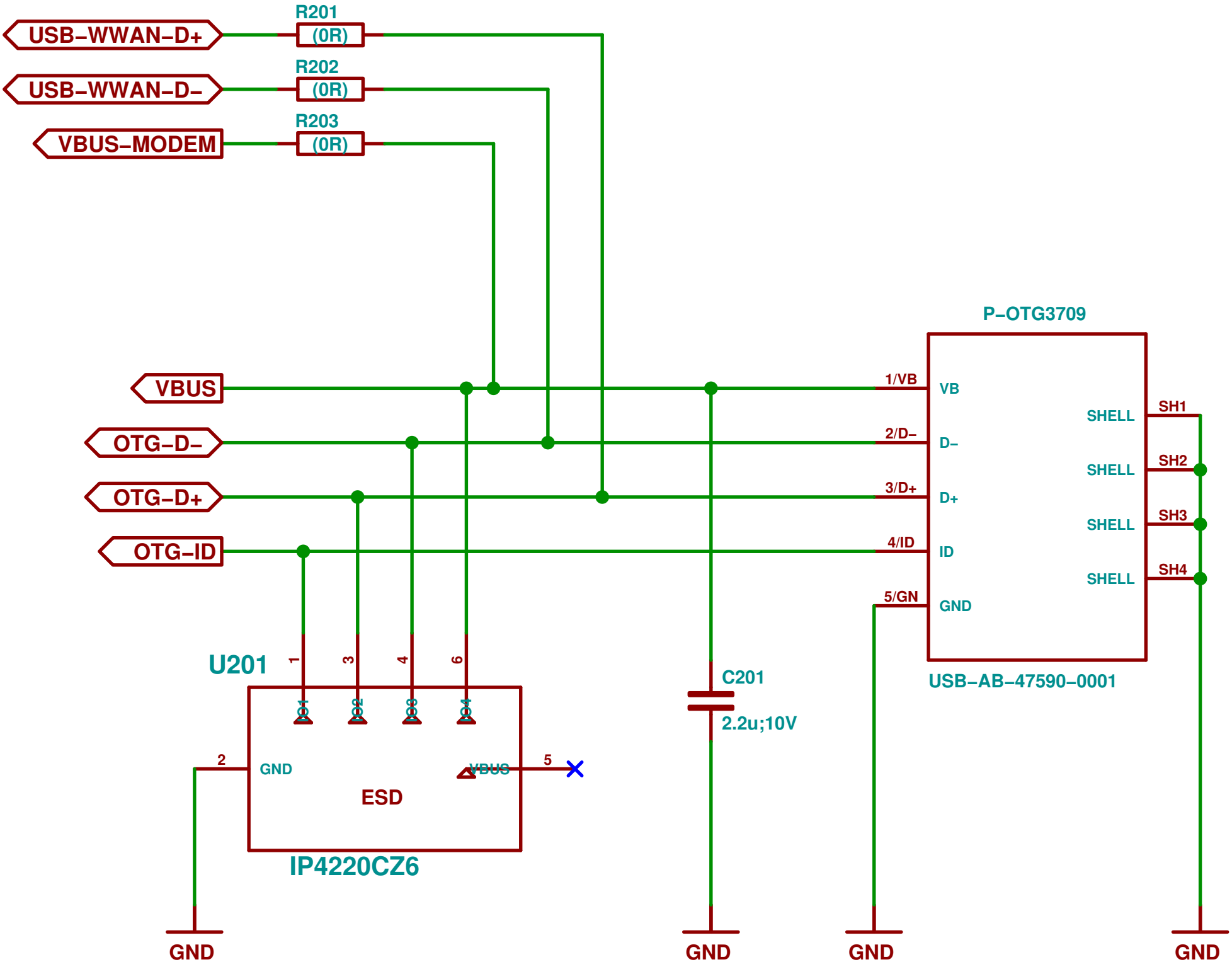


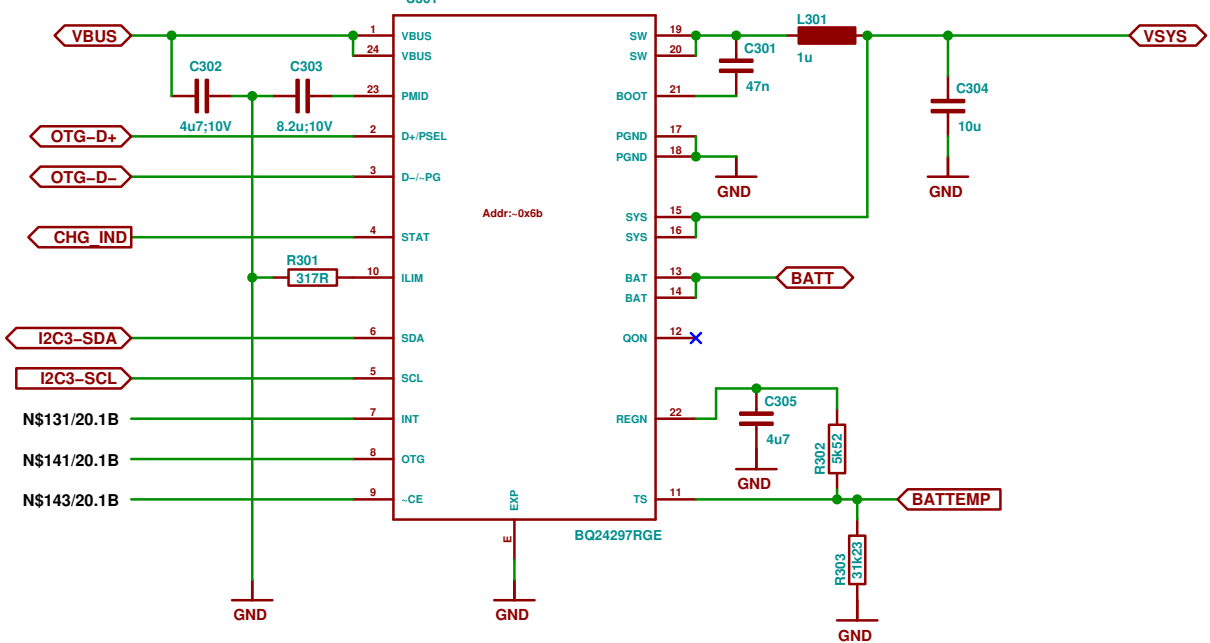
camera trigger



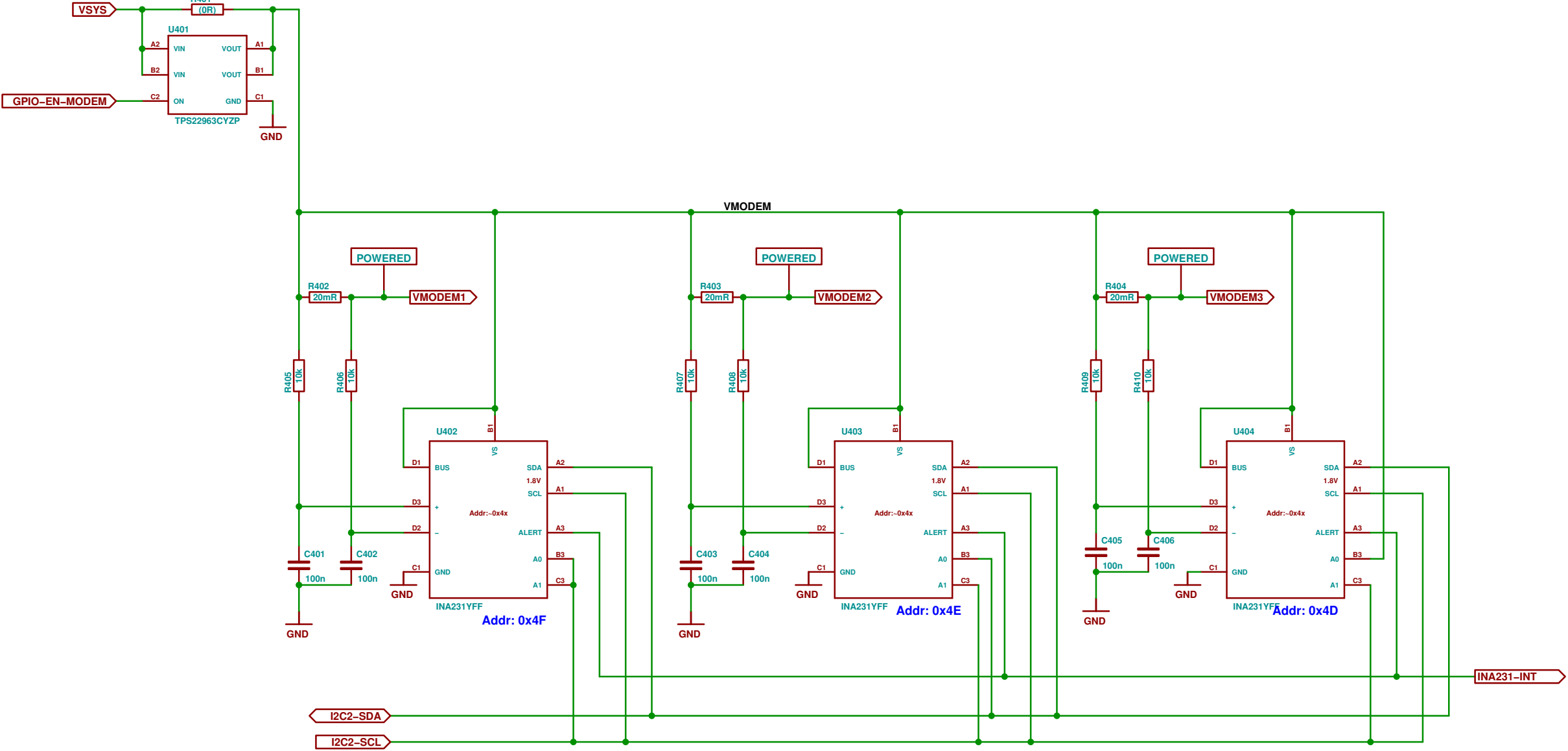
place in scan matrix? would need 3–4 wires to UPPER board instead of 2~
No. VOL+ or VOL– can either be connected to GPIOs
or drive two FETs that sit in the keyboard matrix
in any case it is sufficient to connect GPIO–VOL+ and VOL– to two pins on the B2B connector

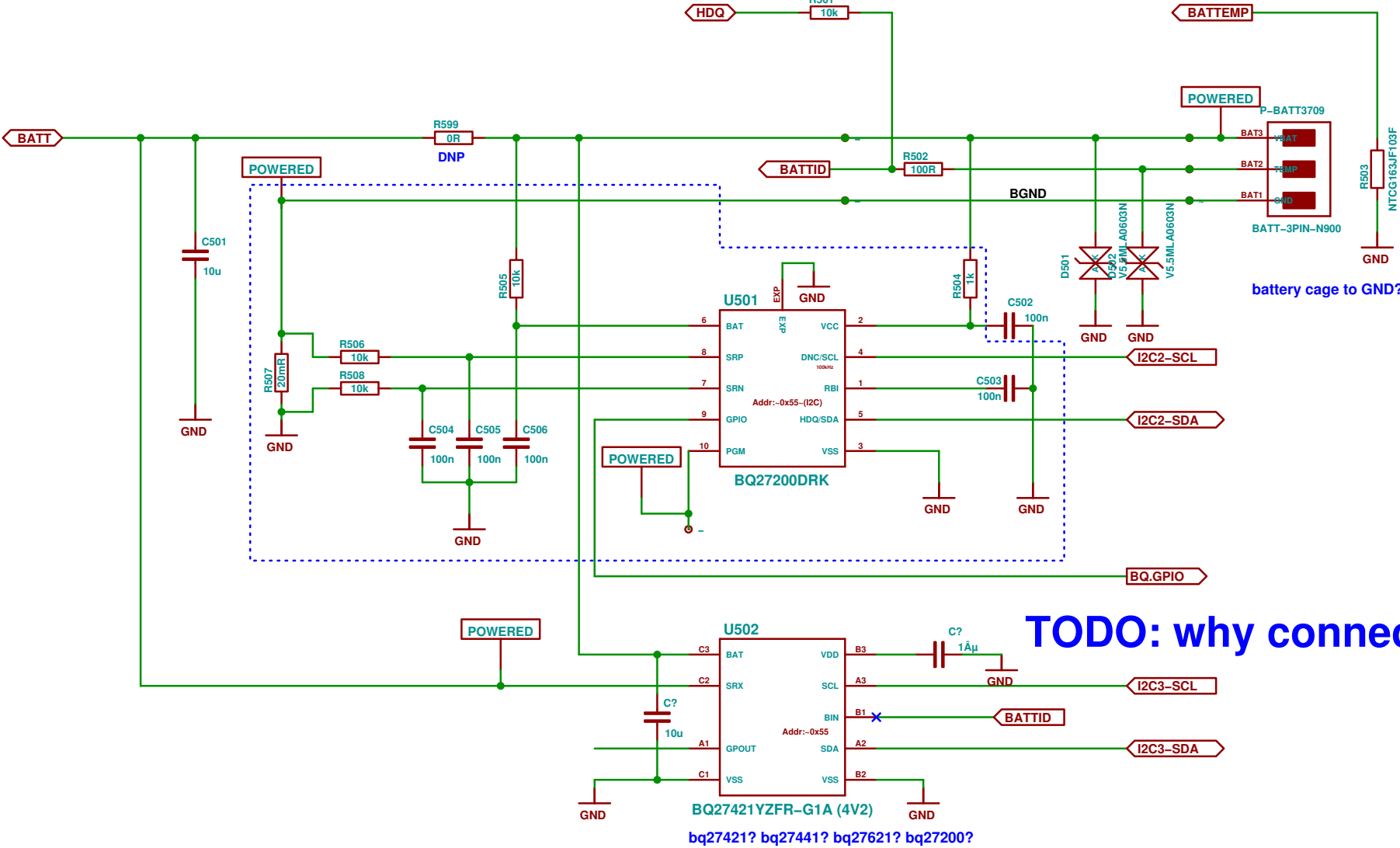
can be used to test/operate the modem through the OTG port (w/o SPPER PCB)

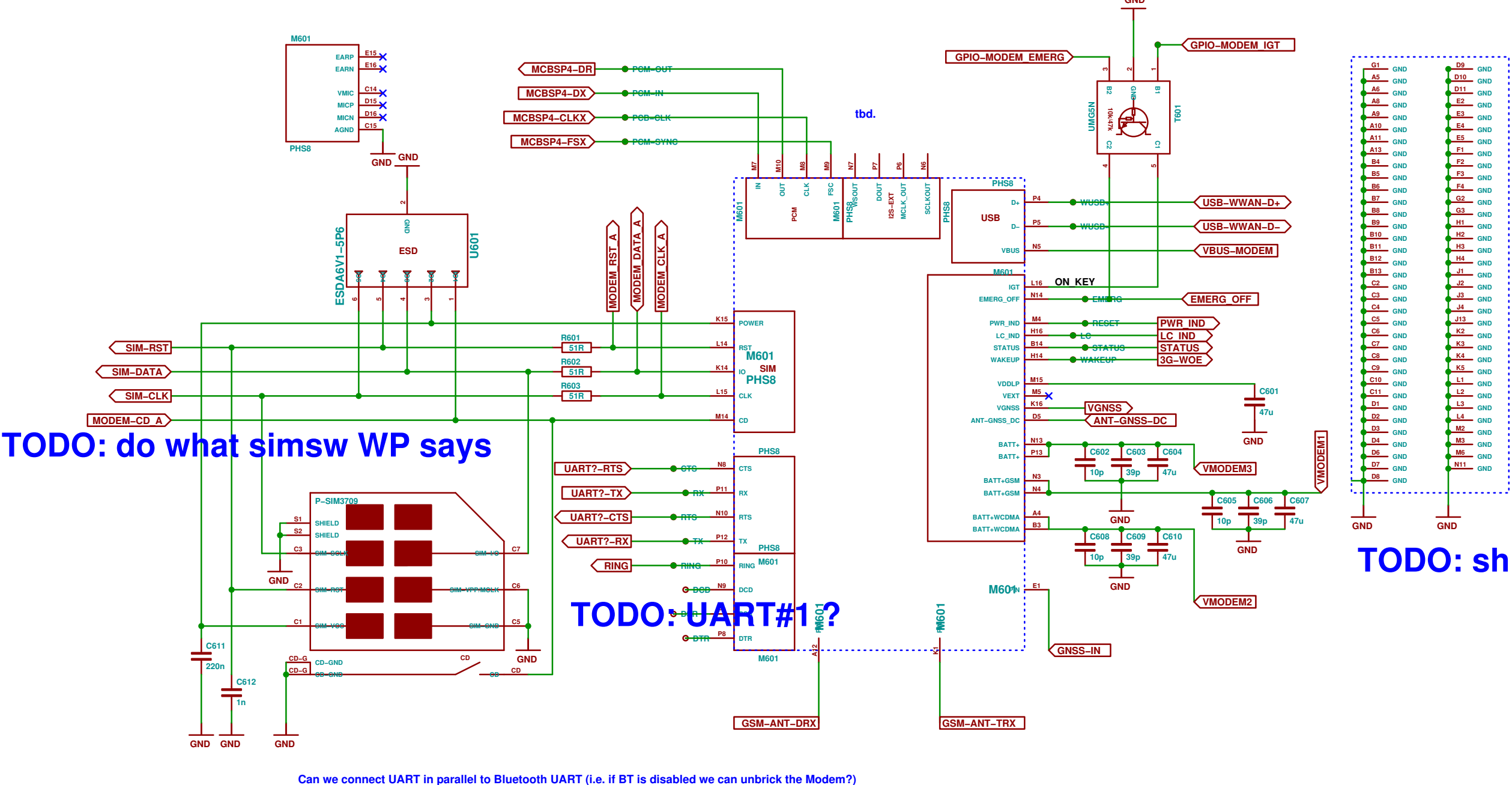


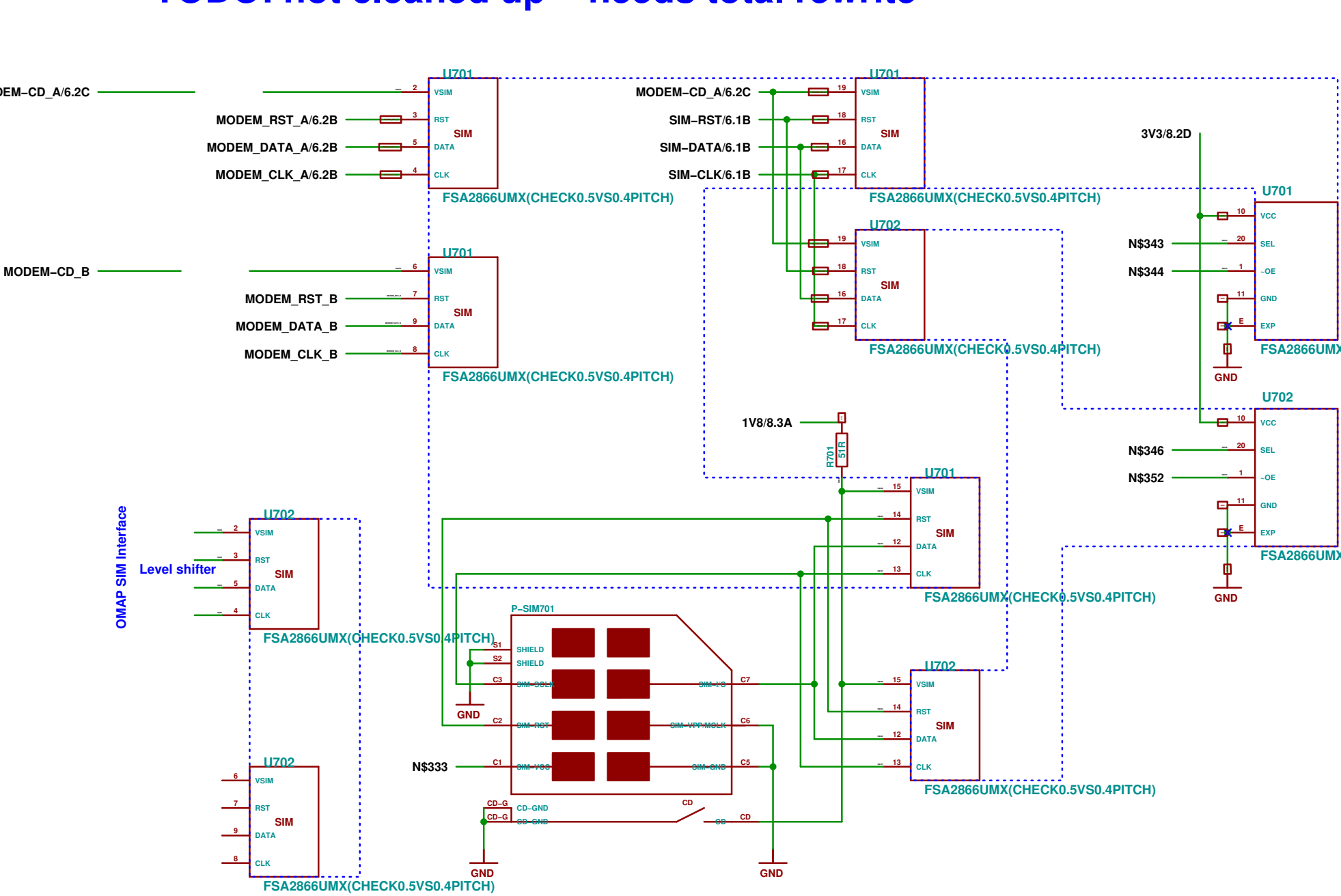

U301
VBUS
C302
C303
4u7;10V
8.2u;10V
OTG-D+
OTG-D-
CHG_IND
R301
317R
I2C3-SDA
I2C3-SCL
N$131/20.1B
N$141/20.1B
N$143/20.1B
1 VBUS
24 VBUS
23 PMID
2 D+/PSEL
3 D-/~PG
4 STAT
10 ILIM
6 SDA
5 SCL
7 INT
8 OTG
9 ~CE
EXP
Addr:-0x6b
19 SW
20 SW
21 BOOT
17 PGND
18 PGND
15 SYS
16 SYS
13 BAT
14 BAT
12 QON
22 REGN
11 TS
L301
1u
C301
47n
C304
10u
BATT
C305
4u7
R302
5k52
R303
31k23
BATTEMP
VSYS
GND
BQ24297RGE

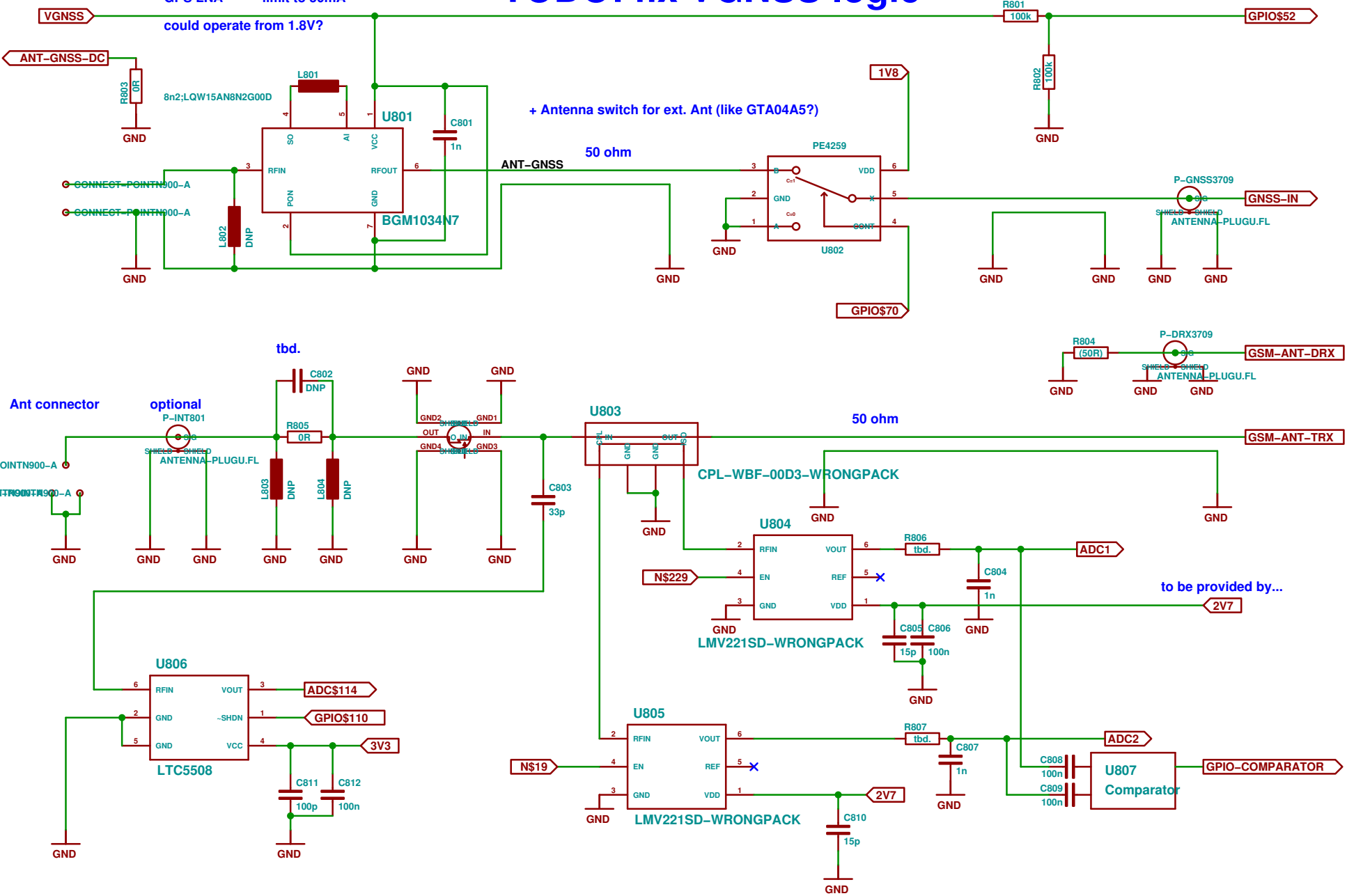
TODO

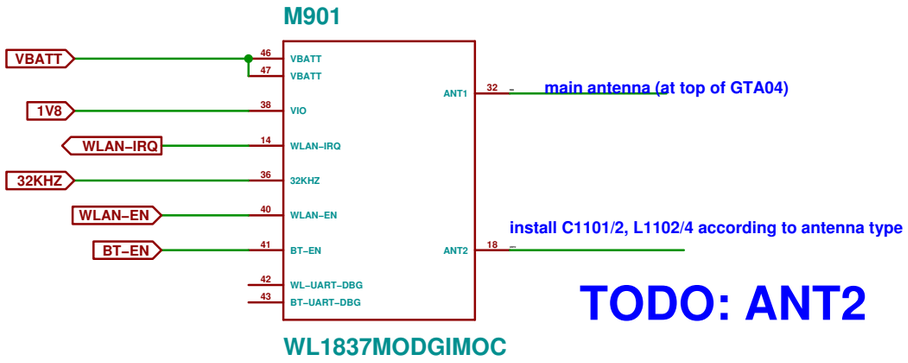

VSYS
R401
(0R)
U401
A2
VIN
VOUT
A1
B2
VIN
VOUT
B1
GPIO-EN-MODEM
C2
ON
GND
C1
TPS22963CYZP
GND
VMODEM
POWERED
R402
20mR
VMODEM1
R405
10k
R406
10k
U402
B1
VS
D1
BUS
SDA
A2
1.8V
A1
D3
SCL
Addr:-0x4x
D2
ALERT
A3
A0
B3
C1
GND
A1
C3
INA231YFF
Addr: 0x4F
C401
100n
C402
100n
GND
GND
POWERED
R403
20mR
VMODEM2
R407
10k
R408
10k
U403
B1
VS
D1
BUS
SDA
A2
1.8V
A1
D3
SCL
Addr:-0x4x
D2
ALERT
A3
A0
B3
C1
GND
A1
C3
INA231YFF
Addr: 0x4E
C403
100n
C404
100n
GND
GND
POWERED
R404
20mR
VMODEM3
R409
10k
R410
10k
U404
B1
VS
D1
BUS
SDA
A2
1.8V
A1
D3
SCL
Addr:-0x4x
D2
ALERT
A3
A0
B3
C1
GND
A1
C3
INA231YFF
Addr: 0x4D
C405
100n
C406
100n
GND
GND
INA231-INT
I2C2-SDA
I2C2-SCL


HDQ
10k
BATTEMP
POWERED
P-BATT3709
BAT3
BAT2
BAT1
VBAT
TEMP
GND
BATT-3PIN-N900
NTCG163JF103F
R503
GND
battery cage to GND?
BATT
R599
0R
DNP
BATTID
R502
100R
BGND
C501
10u
GND
POWERED
R505
10k
R504
1k
D501
D502
V5.5MLA0603N
V5.5MLA0603N
GND
GND
U501
EXP
GND
C502
100n
R506
10k
R508
10k
R507
20mR
GND
C504
100n
C505
100n
C506
100n
GND
BAT
VCC
SRP
DNC/SCL
100kHz
SRN
RBI
Addr:-0x55~(I2C)
GPIO
HDQ/SDA
PGM
VSS
C503
100n
I2C2-SCL
I2C2-SDA
POWERED
GND
GND
BQ27200DRK
BQ.GPIO
TODO: why connec
POWERED
U502
C?
1Âµ
GND
BAT
VDD
SRX
SCL
I2C3-SCL
C?
10u
BIN
BATTID
Addr:-0x55
GPOUT
SDA
I2C3-SDA
VSS
VSS
GND
GND
BQ27421YZFR-G1A (4V2)
bq27421? bq27441? bq27621? bq27200?
TODO: can U501 and U502 coexist ?
TODO: BQ27421YZFR-G1A


M601
EARP
EARN
VMIC
MICP
MICN
AGND
PHS8
GND
ESD
ESDA6V1-5P6
U601
MODEM_RST_A
MODEM_DATA_A
MODEM_CLK_A
MCBSP4-DR
MCBSP4-DX
MCBSP4-CLKX
MCBSP4-FSX
PCM-OUT
PCM-IN
PCB-CLK
PCM-SYNC
tbd.
PCM
I2S-EXT
GPIO-MODEM_EMERG
GPIO-MODEM_IGT
UMG5N
T601
USB
USB-WWAN-D+
USB-WWAN-D-
VBUS-MODEM
ON_KEY
EMERG_OFF
PWR_IND
LC_IND
STATUS
3G-WOE
VGNSS
ANT-GNSS-DC
VMODEM1
VMODEM3
VMODEM2
SIM-RST
SIM-DATA
SIM-CLK
MODEM-CD_A
R601
R602
R603
51R
P-SIM3709
UART?-RTS
UART?-TX
UART?-CTS
UART?-RX
RING
GSM-ANT-DRX
GSM-ANT-TRX
GNSS-IN
TODO: do what simsw WP says
TODO: UART#1?
TODO: sh
Can we connect UART in parallel to Bluetooth UART (i.e. if BT is disabled we can unbrick the Modem?)

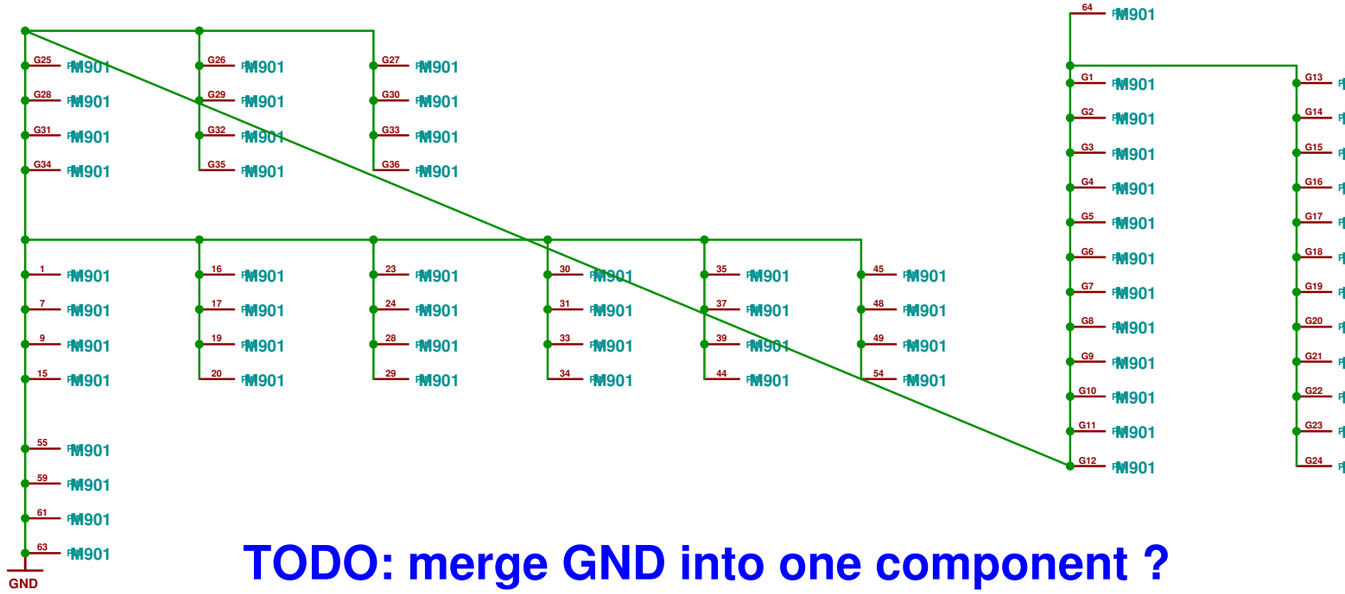

NOT cleaned up - needs total rewrite
U701
VSIM
RST
DATA
CLK
SIM
MODEM_RST_A/6.2B
MODEM_DATA_A/6.2B
MODEM_CLK_A/6.2B
FSA2866UMX(CHECK0.5VS0.4PITCH)
MODEM_CD_A/6.2C
SIM_RST/6.1B
SIM_DATA/6.1B
SIM_CLK/6.1B
U702
MODEM_CD_B
MODEM_RST_B
MODEM_DATA_B
MODEM_CLK_B
3V3/8.2D
N$343
N$344
VCC
SEL
-OE
GND
EXP
N$346
N$352
1V8/8.3A
R701
51R
OMAP SIM Interface
Level shifter
P-SIM701
SHIELD
SIM_SCLK
SIM_RST
SIM_VCC
SIM_I/O
SIM_VPP/MCLK
SIM_GND
CD-G
CD-GND
CD
N$333
NOTE: mux control missingnNOTE: CD logic missingnNOTE: SIM power supply missing


TODO: fix VGNSS logic
VGNSS
could operate from 1.8V?
R801
100k
GPIO$52
R802
100k
GND
ANT-GNSS-DC
R803
0R
L801
8n2;LQW15AN8N2G00D
U801
C801
1n
+ Antenna switch for ext. Ant (like GTA04A5?)
50 ohm
1V8
PE4259
U802
P-GNSS3709
GNSS-IN
ANTENNA-PLUGU.FL
CONNECT-POINTN900-A
CONNECT-POINTN900-A
L802
DNP
BGM1034N7
ANT-GNSS
GPIO$70
tbd.
C802
DNP
R804
(50R)
P-DRX3709
GSM-ANT-DRX
Ant connector
optional
P-INT801
R805
0R
ANTENNA-PLUGU.FL
L803
DNP
L804
DNP
C803
33p
U803
50 ohm
GSM-ANT-TRX
CPL-WBF-00D3-WRONGPACK
U804
R806
tbd.
ADC1
N$229
C804
1n
to be provided by...
2V7
C805
15p
C806
100n
LMV221SD-WRONGPACK
U806
ADC$114
GPIO$110
3V3
LTC5508
C811
100p
C812
100n
U805
R807
tbd.
ADC2
N$19
C807
1n
C808
100n
C809
100n
U807
Comparator
GPIO-COMPARATOR
C810
15p
LMV221SD-WRONGPACK
GND
TODO: name all the *$*



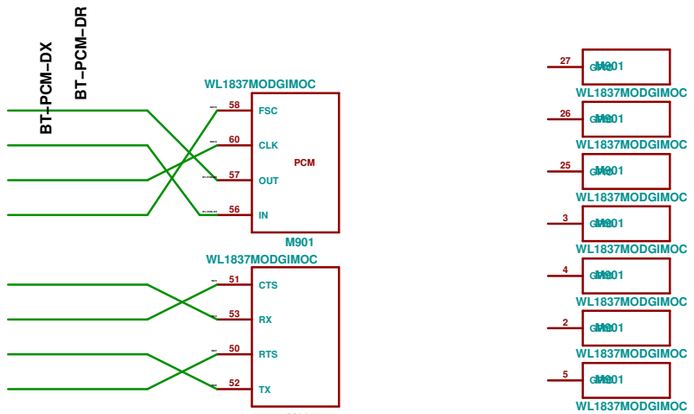
TODO: ANT2

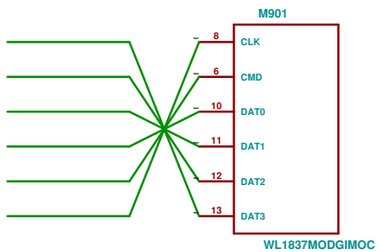
secondary (on the side of GTA04)ncould be 5.8GHz as well



TODO: merge GND into one component ?

TODO: unfinished



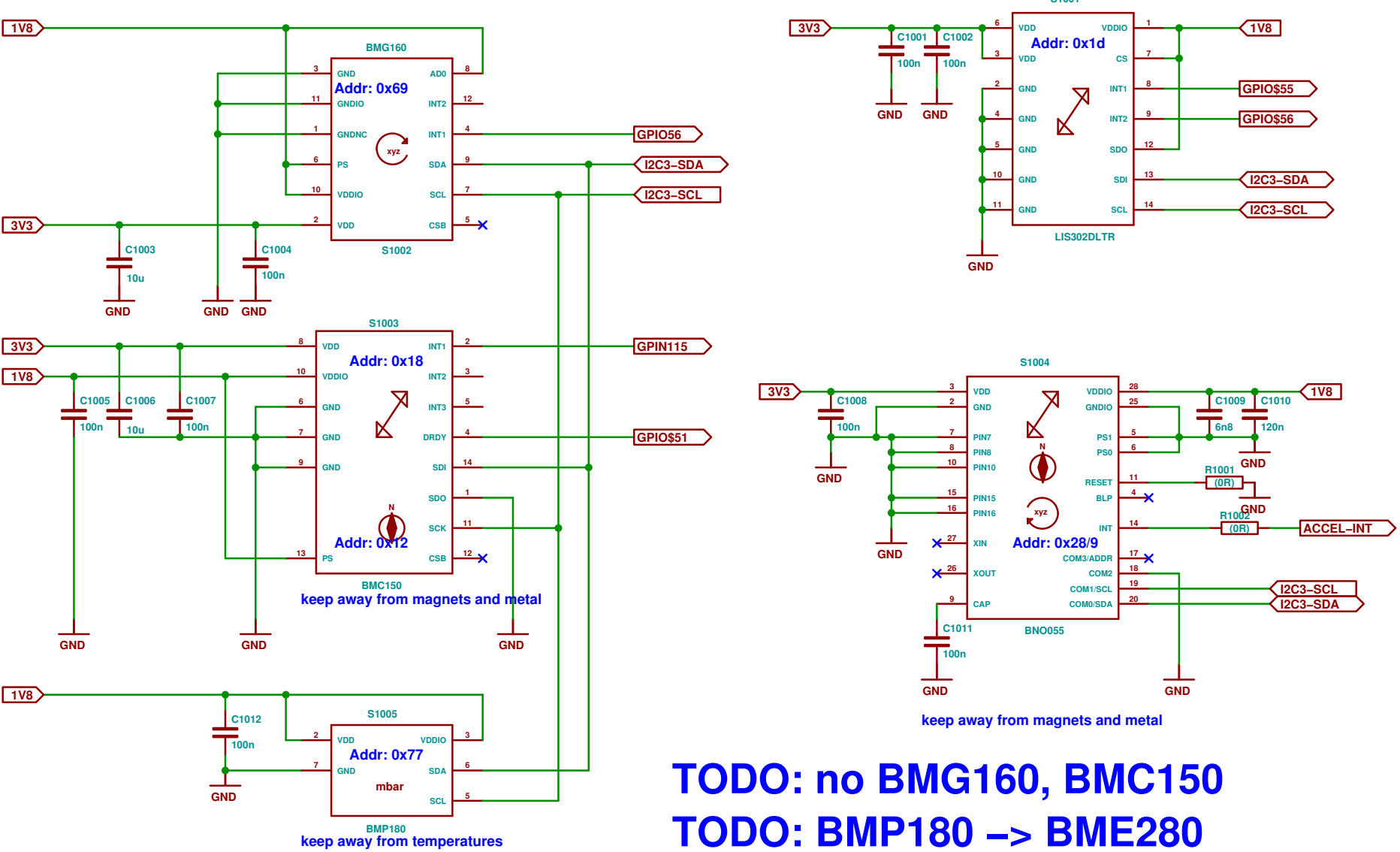


WLAN-IRQ
WLAN-EN
BT-EN
GPIO175
KEYIRQ

Si4705 is pin compatible (mostly) but RX-only

TODO: unfinished

FSX
CLK
DX
DR
FSR
CLK



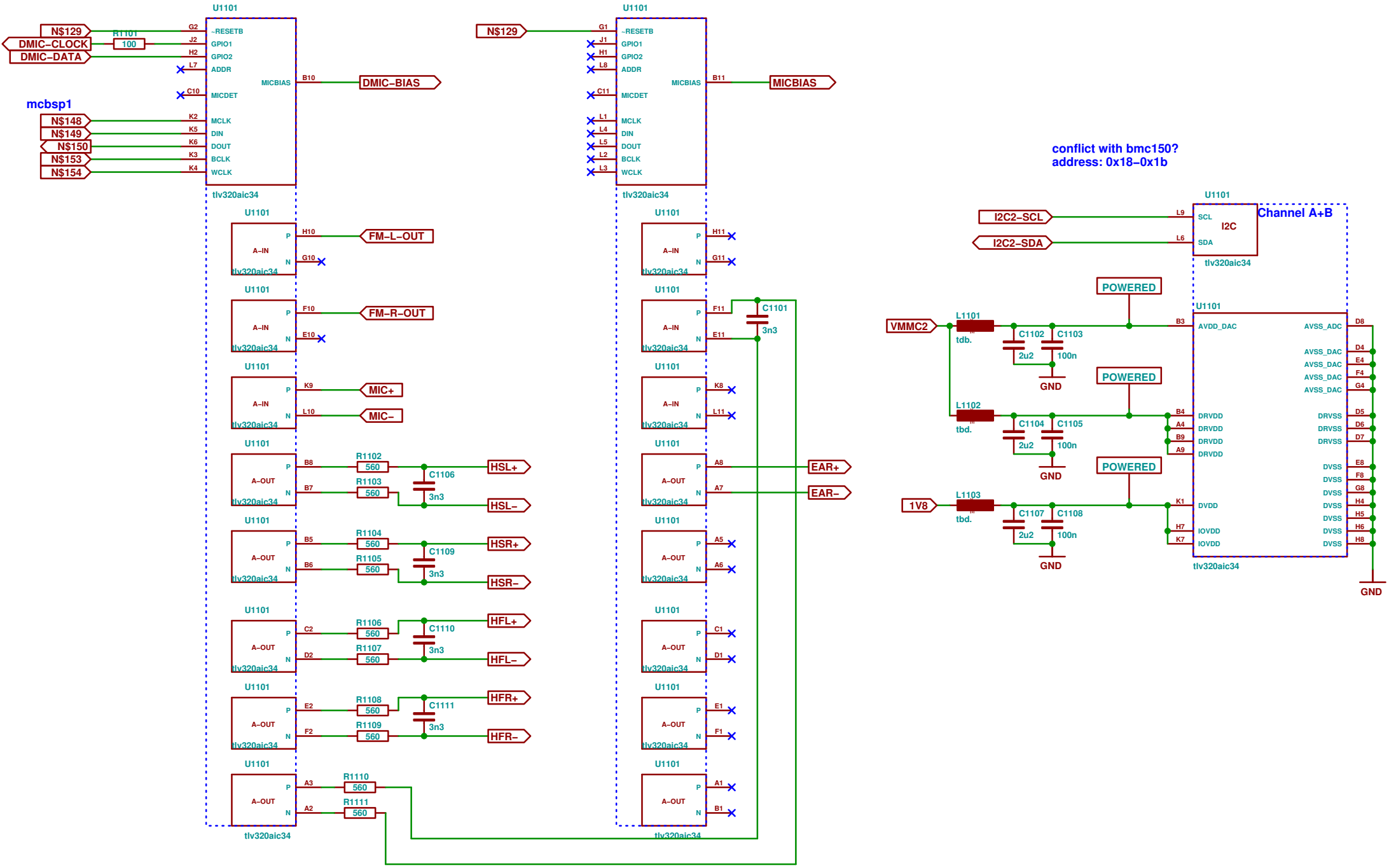
TODO: no BMG160, BMC150

TODO: BMP180 –> BME280

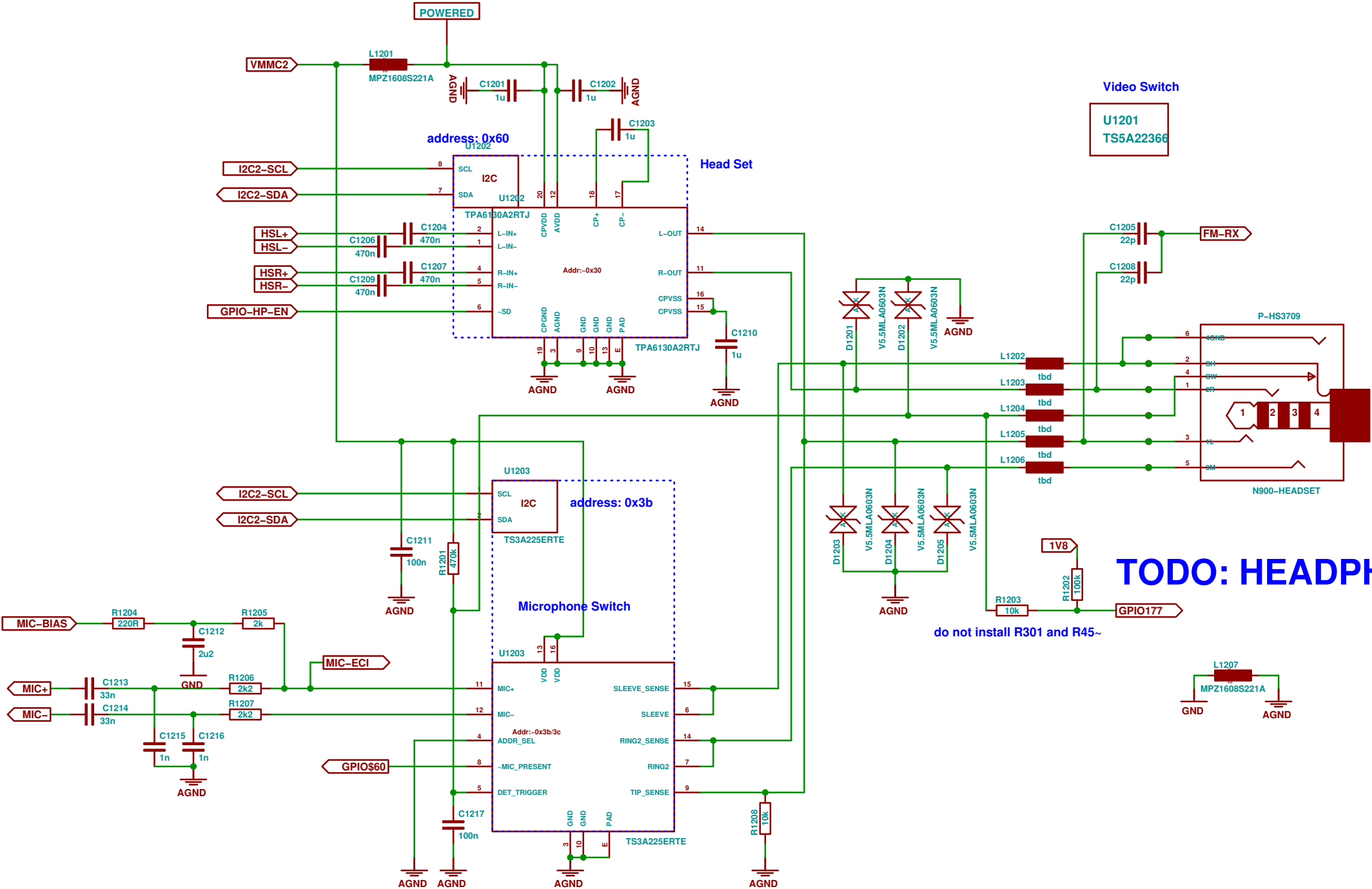
TODO: BNO055 –> BMX055

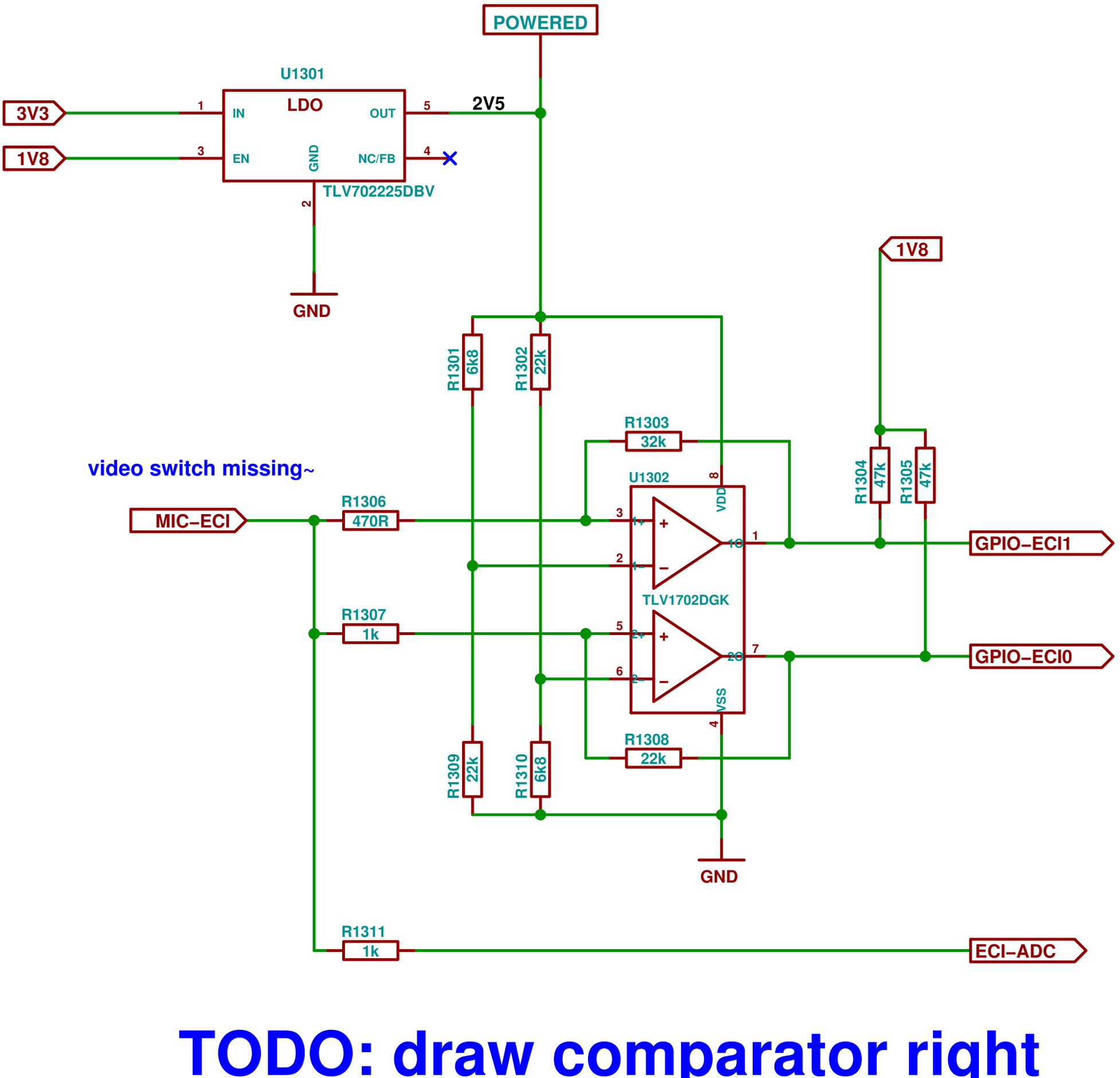
TODO: INT1/2 sharing

problem: this is a 0.5mm BGA making lower board expensive~
but it appears to be not extremely critical (only 3 rows and inner ring is GND)
problem: analog mic is on upper board~
alternative: place on upper board (to be evaluated)

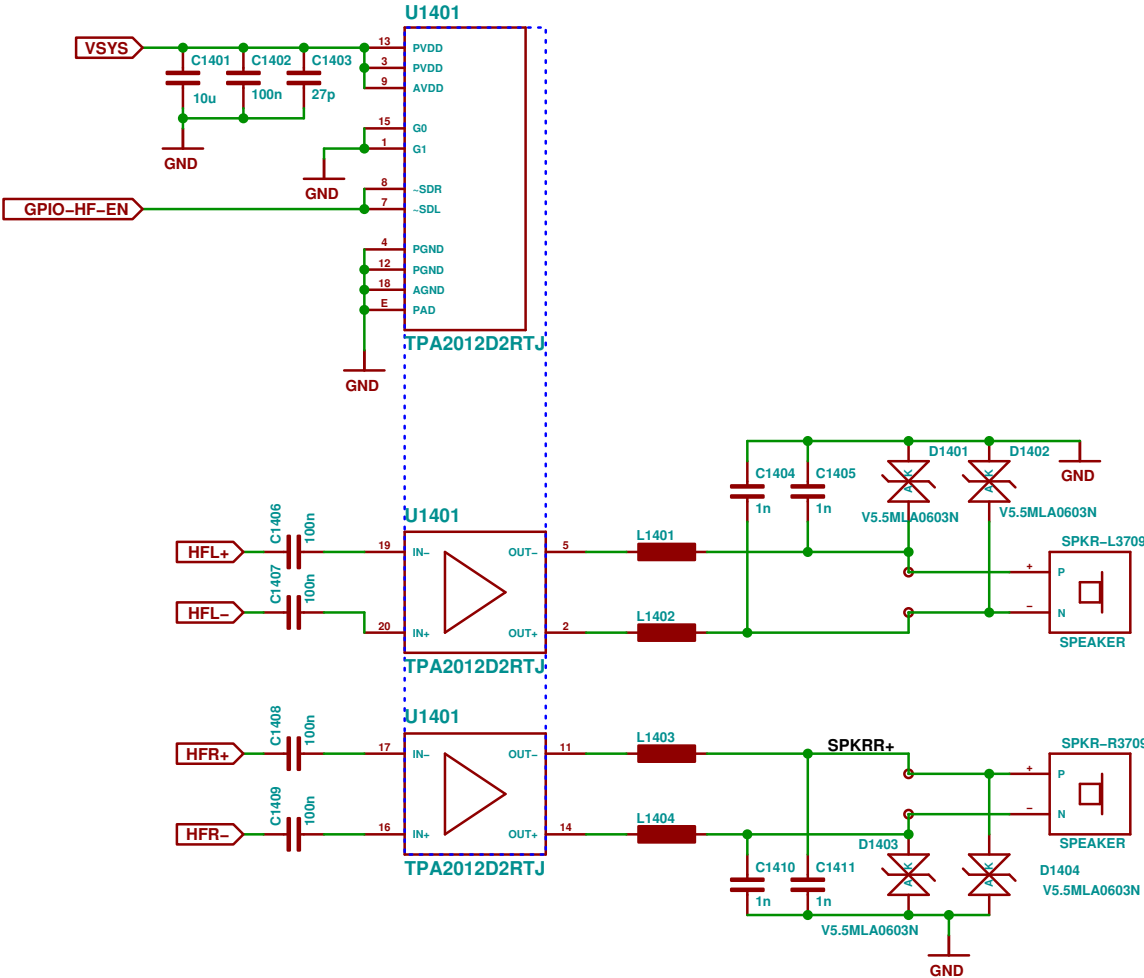


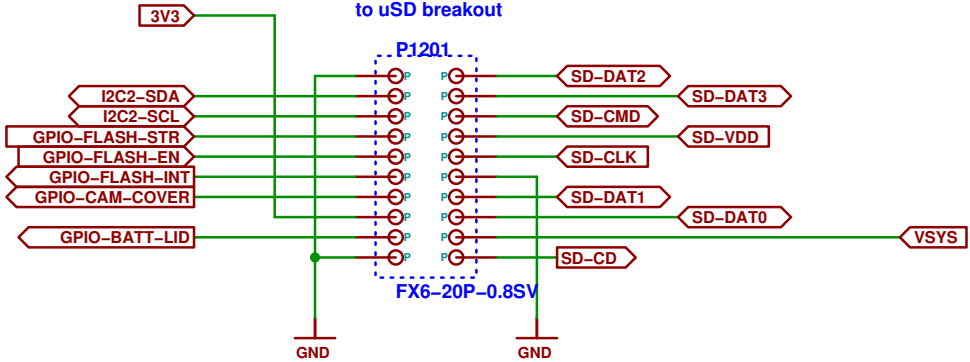
conflict with bmc150?
address: 0x18-0x1b


POWERED
VMMC2
L1201
MPZ1608S221A
AGND
C1201
1u
C1202
1u
C1203
1u
address: 0x60
U1202
I2C
SCL
SDA
TPA6130A2RTJ
Head Set
I2C2-SCL
I2C2-SDA
HSL+
HSL-
HSR+
HSR-
GPIO-HP-EN
C1204
470n
C1206
470n
C1207
470n
C1209
470n
L-IN+
L-IN-
R-IN+
R-IN-
~SD
L-OUT
R-OUT
CPVSS
CPGND
AGND
GND
PAD
Addr:-0x30
C1210
1u
Video Switch
U1201
TS5A22366
C1205
22p
C1208
22p
FM-RX
P-HS3709
N900-HEADSET
D1201
D1202
D1203
D1204
D1205
V5.5MLA0603N
L1202
L1203
L1204
L1205
L1206
tbd
U1203
address: 0x3b
TS3A225ERTE
C1211
100n
R1201
470k
Microphone Switch
MIC-BIAS
R1204
220R
R1205
2k
C1212
2u2
MIC-ECI
MIC+
MIC-
C1213
33n
C1214
33n
R1206
2k2
R1207
2k2
C1215
1n
C1216
1n
GPIO$60
C1217
100n
Addr:-0x3b/3c
MIC+
MIC-
ADDR_SEL
~MIC_PRESENT
DET_TRIGGER
SLEEVE_SENSE
SLEEVE
RING2_SENSE
RING2
TIP_SENSE
R1208
10k
1V8
R1202
100k
R1203
10k
GPIO177
do not install R301 and R45~
TODO: HEADPH
L1207
MPZ1608S221A
GND

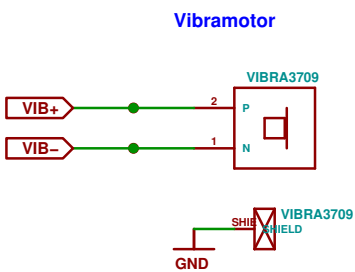


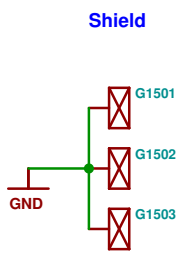
TODO: draw comparator right

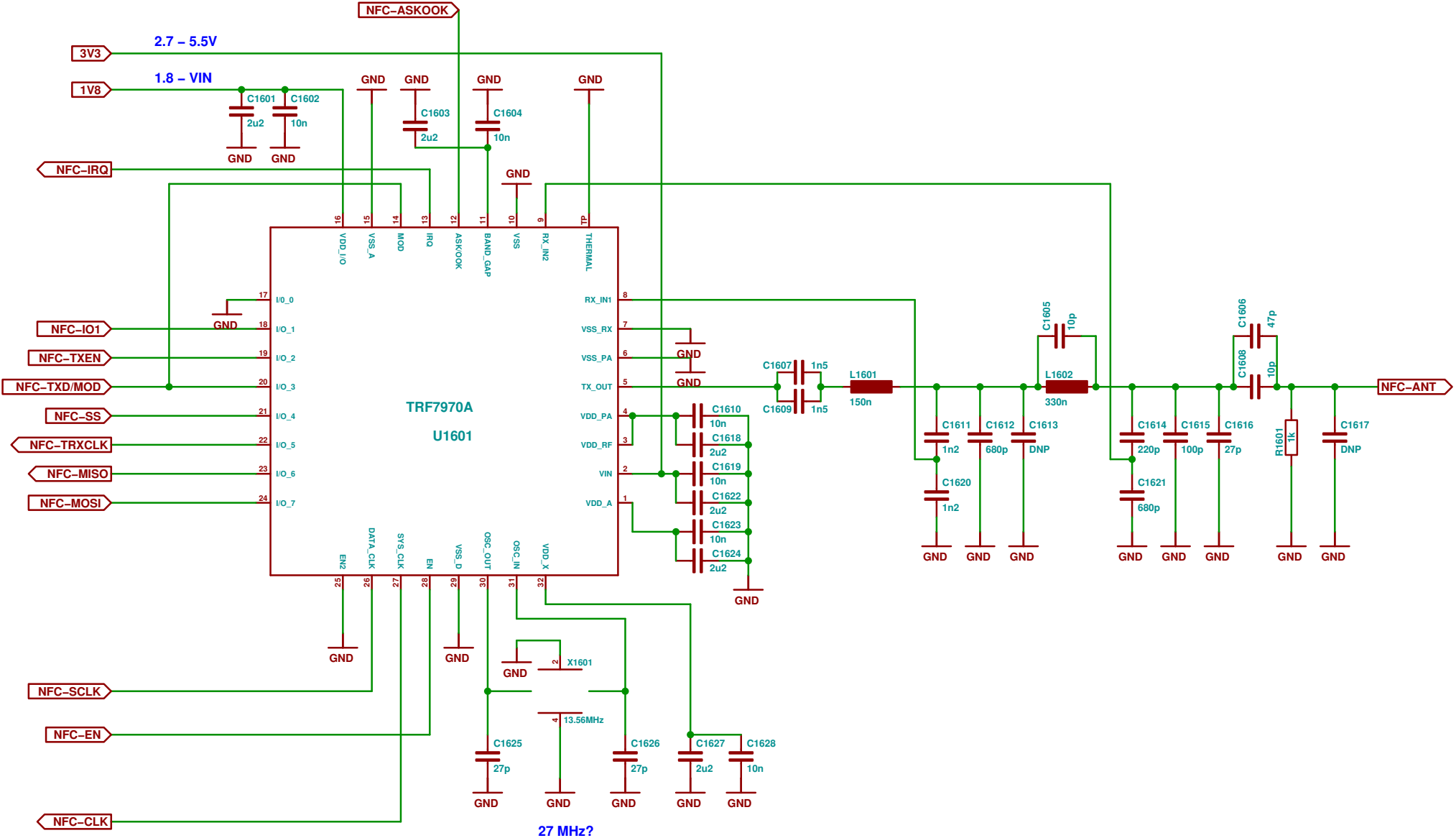

U1401
VSYS
C1401
C1402
C1403
10u
100n
27p
GND
13
3
9
PVDD
PVDD
AVDD
15
1
G0
G1
GND
GPIO-HF-EN
8
7
~SDR
~SDL
4
12
18
E
PGND
PGND
AGND
PAD
TPA2012D2RTJ
GND
U1401
HFL+
HFL-
C1406
C1407
100n
100n
19
20
IN-
IN+
OUT-
OUT+
5
2
L1401
L1402
TPA2012D2RTJ
C1404
C1405
1n
1n
D1401
D1402
V5.5MLA0603N
V5.5MLA0603N
GND
SPKR-L3709
P
N
SPEAKER
U1401
HFR+
HFR-
C1408
C1409
100n
100n
17
16
IN-
IN+
OUT-
OUT+
11
14
L1403
L1404
SPKRR+
TPA2012D2RTJ
C1410
C1411
1n
1n
D1403
D1404
V5.5MLA0603N
V5.5MLA0603N
GND
SPKR-R3709
P
N
SPEAKER

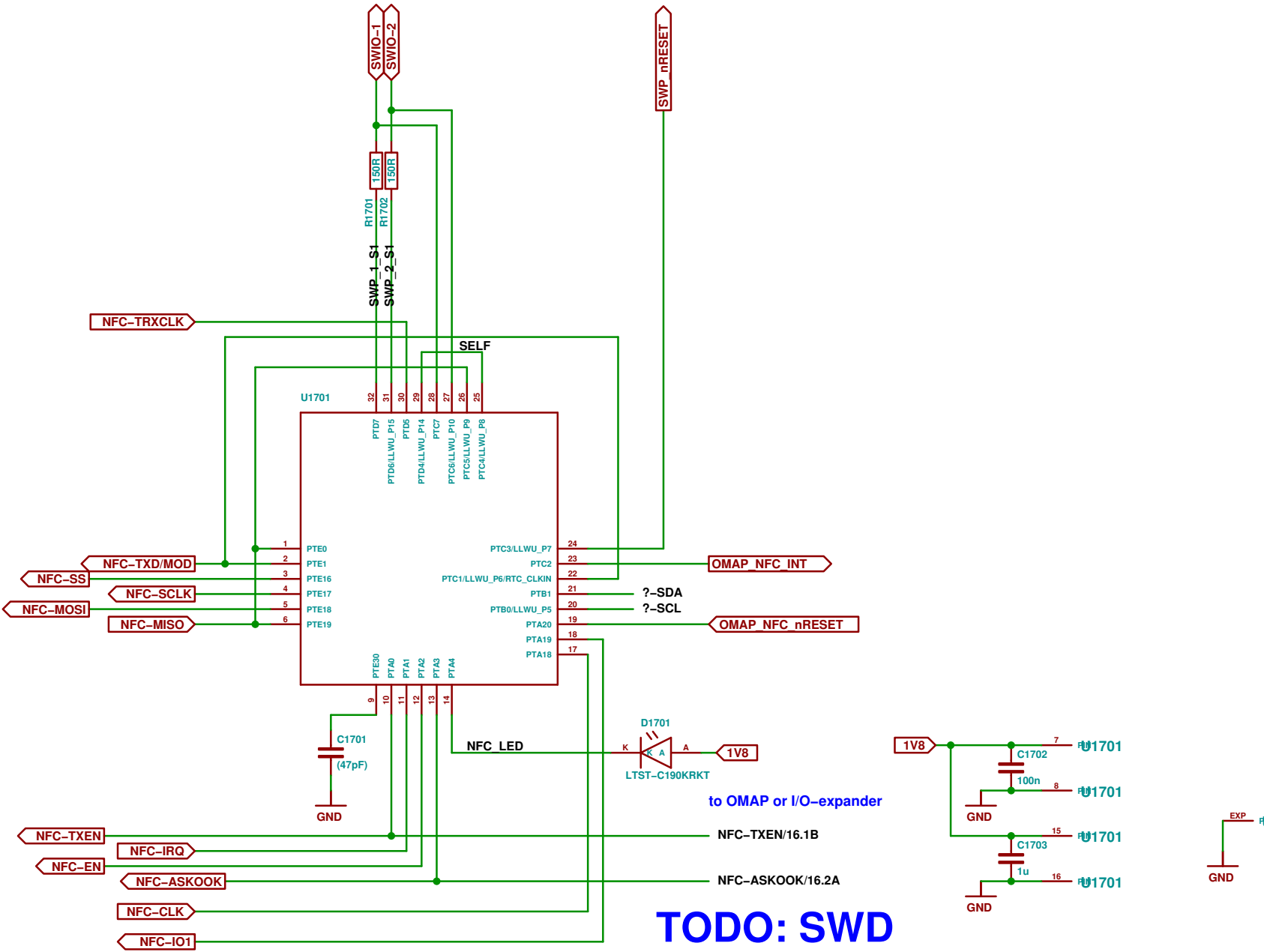


TODO: bogus connector (see HB WP)

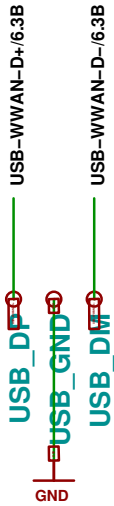




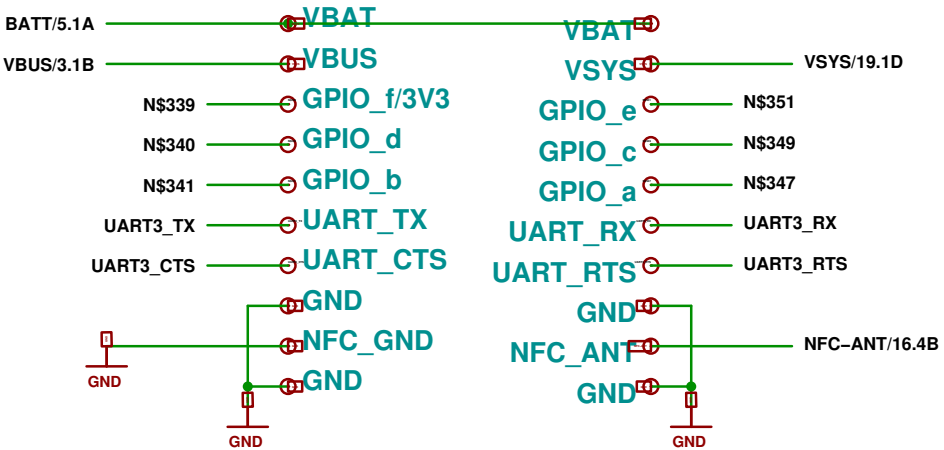

NFC-ASKOOK
3V3
2.7 – 5.5V
1V8
1.8 – VIN
C1601
2u2
C1602
10n
C1603
2u2
C1604
10n
GND
NFC-IRQ
TRF7970A
U1601
VDD_I/O
VSS_A
MOD
IRQ
ASKOOK
BAND_GAP
VSS
RX_IN2
THERMAL
I/O_0
I/O_1
I/O_2
I/O_3
I/O_4
I/O_5
I/O_6
I/O_7
RX_IN1
VSS_RX
VSS_PA
TX_OUT
VDD_PA
VDD_RF
VIN
VDD_A
NFC-IO1
NFC-TXEN
NFC-TXD/MOD
NFC-SS
NFC-TRXCLK
NFC-MISO
NFC-MOSI
C1607
1n5
C1609
1n5
L1601
150n
C1605
10p
L1602
330n
C1606
47p
C1608
10p
NFC-ANT
C1610
10n
C1618
2u2
C1619
10n
C1622
2u2
C1623
10n
C1624
2u2
C1611
1n2
C1620
1n2
C1612
680p
C1613
DNP
C1614
220p
C1621
680p
C1615
100p
C1616
27p
R1601
1k
C1617
DNP
EN2
DATA_CLK
SYS_CLK
EN
VSS_D
OSC_OUT
OSC_IN
VDD_X
X1601
13.56MHz
C1625
27p
C1626
27p
C1627
2u2
C1628
10n
NFC-SCLK
NFC-EN
NFC-CLK
27 MHz?


SWIO-1
SWIO-2
SWP_nRESET
150R
150R
R1701
R1702
SWP_1_S1
SWP_2_S1
NFC-TRXCLK
SELF
U1701
32
31
30
29
28
27
26
25
PTD7
PTD6/LLWU_P15
PTD5
PTD4/LLWU_P14
PTC7
PTC6/LLWU_P10
PTC5/LLWU_P9
PTC4/LLWU_P8
1
2
3
4
5
6
PTE0
PTE1
PTE16
PTE17
PTE18
PTE19
NFC-TXD/MOD
NFC-SS
NFC-SCLK
NFC-MOSI
NFC-MISO
PTC3/LLWU_P7
PTC2
PTC1/LLWU_P6/RTC_CLKIN
PTB1
PTB0/LLWU_P5
PTA20
PTA19
PTA18
24
23
22
21
20
19
18
17
OMAP_NFC_INT
?-SDA
?-SCL
OMAP_NFC_nRESET
PTE30
PTA0
PTA1
PTA2
PTA3
PTA4
9
10
11
12
13
14
C1701
(47pF)
GND
NFC_LED
D1701
K
A
LTST-C190KRKT
1V8
to OMAP or I/O-expander
NFC-TXEN
NFC-IRQ
NFC-EN
NFC-ASKOOK
NFC-CLK
NFC-IO1
NFC-TXEN/16.1B
NFC-ASKOOK/16.2A
TODO: SWD
1V8
C1702
100n
C1703
1u
GND
U1701
7
8
15
16
EXP

NOTE: this is mangling up Breakout and Lower board connectorsh!Signals may have to be fed through the breakout board connector increas



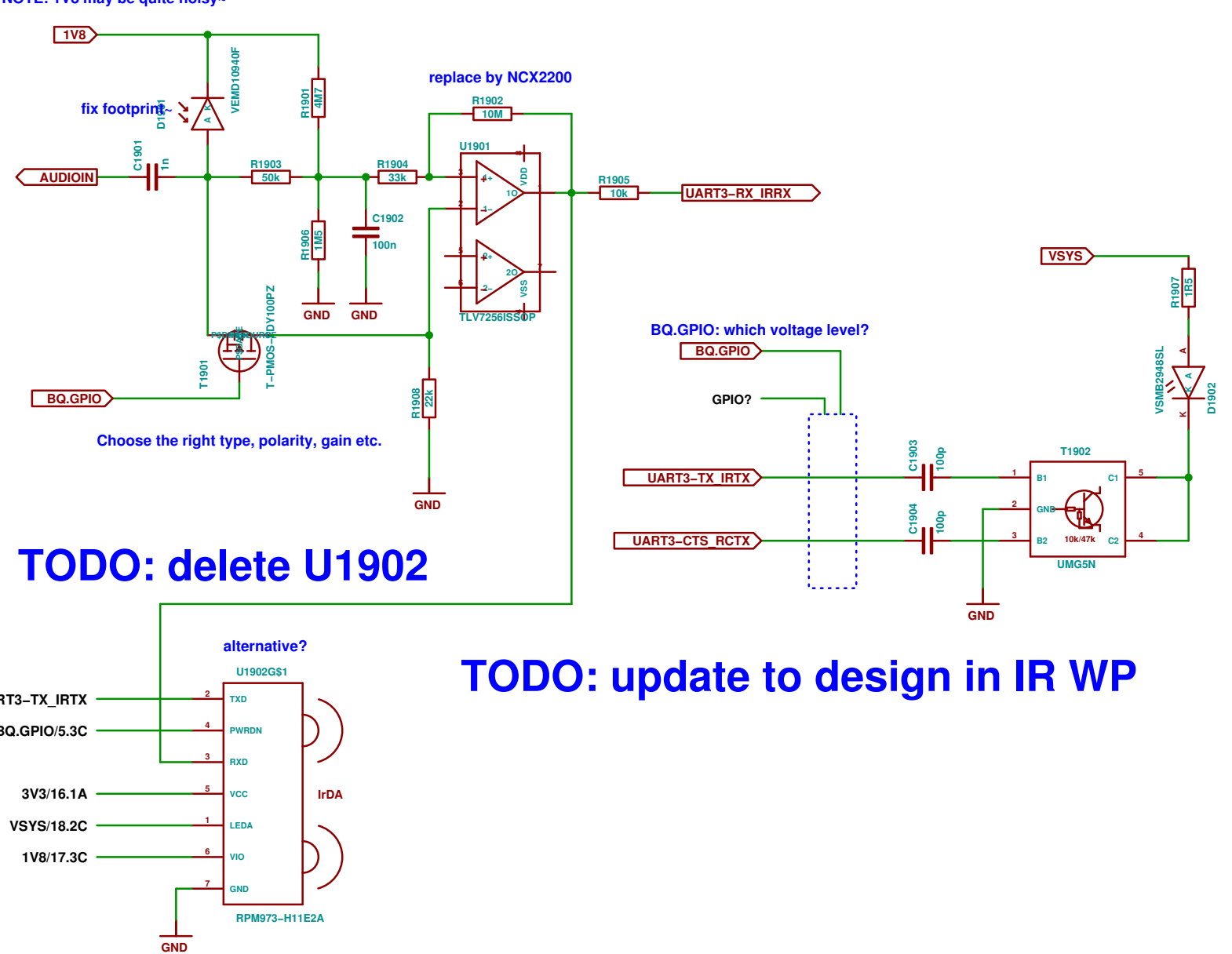
TODO: align with HB WP



Missing 10 level shifter chip (or do we really have the space for 10x discrete T+R+D ca. 3x3mm each?)

Missing 6x 2R for alternate function select (do we have the space for ca. 2.5 x 5mm?)

TODO: align with HB WP


1V8
fix footprint~
D1901
VEMD10940F
R1901
4M7
replace by NCX2200
R1902
10M
U1901
C1901
1n
AUDIOIN
R1903
50k
R1904
33k
R1905
10k
UART3-RX_IRRX
R1906
1M5
C1902
100n
GND
GND
VDD
VSS
TLV7256ISSOP
T1901
T-PMOS-SOT100PZ
BQ.GPIO
R1908
22k
GND
Choose the right type, polarity, gain etc.
TODO: delete U1902
BQ.GPIO: which voltage level?
BQ.GPIO
GPIO?
UART3-TX_IRTX
UART3-CTS_RCTX
C1903
100p
C1904
100p
T1902
B1
C1
GND
B2
10k/47k
C2
UMG5N
GND
VSYS
R1907
1R5
VSMB2948SL
D1902
TODO: update to design in IR WP
alternative?
U1902G$1
RT3-TX_IRTX
BQ.GPIO/5.3C
3V3/16.1A
VSYS/18.2C
1V8/17.3C
TXD
PWRDN
RXD
VCC
LEDA
VIO
GND
IrDA
RPM973-H11E2A
GND

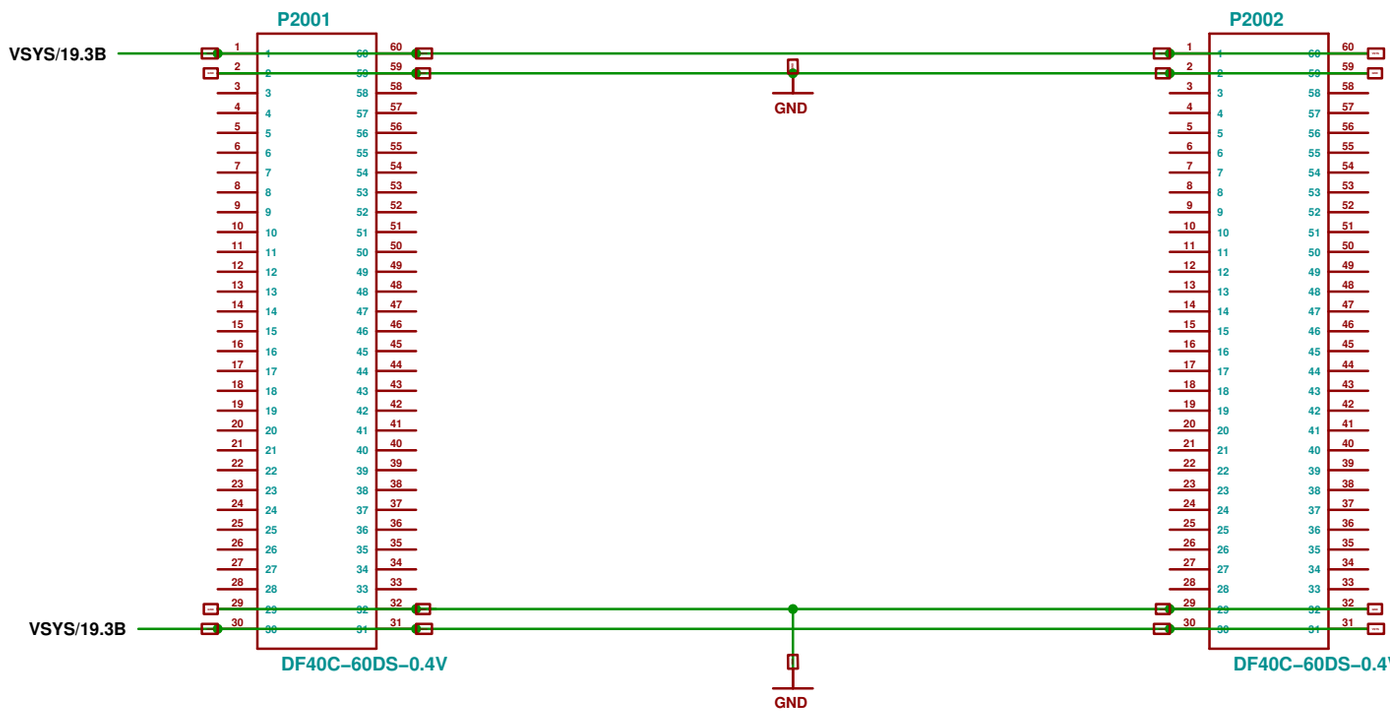
PCB Layout update when details settle

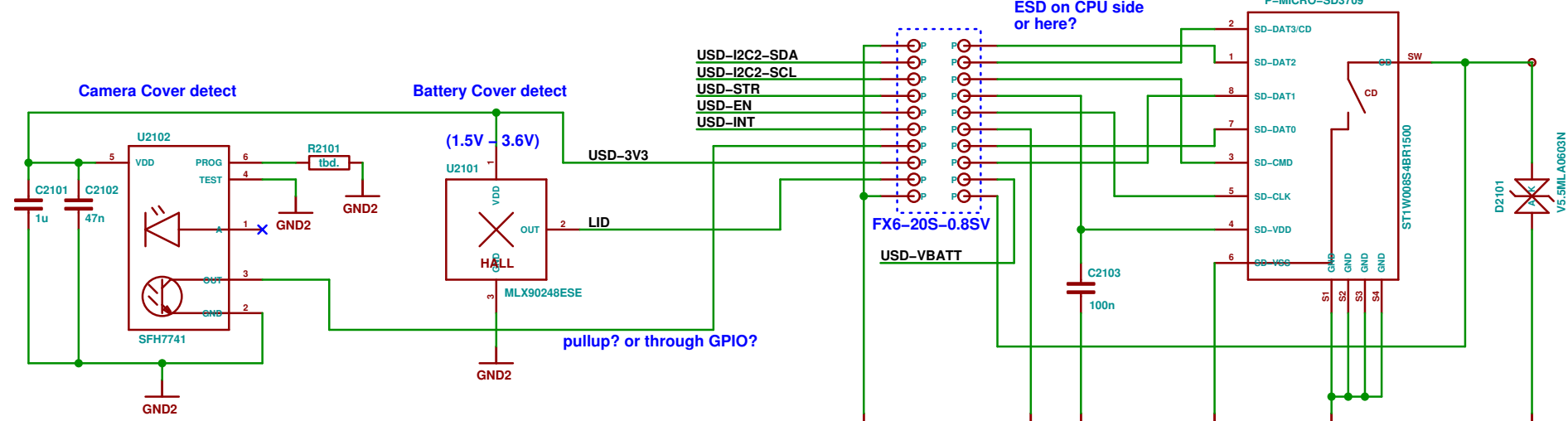
ca. 130 signals (to be counted exactly after definition of upper/lower split)

LOCK–GPIO/1.2A
POWERON/1.3A
GPIO–VOL+/1.2B
GPIO–VOL–/1.2B
CAM1–GPIO/1.3B
CAM2–GPIO/1.3C
I2C3–SDA/10.4C
I2C3–SCL/10.4C
CHG_IND/3.1B
N$131/3.1C
N$141/3.1C
N$143/3.1C
BATTEMP/5.4A
GPIO–EN–MODEM/4.1A
I2C2–SDA/15.1A
I2C2–SCL/15.1A
INA231–INT/4.4C
HDQ/5.2A
GPIO$70/8.3B
GPIO$110/8.1D
N$19/8.2D
N$229/8.3C
ADC$114/8.1C
ADC1/8.4C
ADC2/8.4C
GPIO–COMPARATOR/8.4D
MCBSP4–DR/6.2A
MCBSP4–DX/6.2A
MCBSP4–CLKX/6.2A
MCBSP4–FSX/6.2A
UART?–RTS/6.2C
UART?–CTS/6.2C
UART?–RX/6.2C
UART?–TX/6.2C
RING/6.2C
GPIO–MODEM_IGT/6.3A
GPIO–MODEM_EMERG/6.3A
EMERG_OFF/6.3B
PWR_IND/6.3B
LC_IND/6.3B
STATUS/6.3B
3G–WOE/6.3B
GPIO$52/8.4A
GPIO–WLAN–EN/9.1A
MMC3–CLK/9.1A
MMC3–CMD/9.1A
MMC3–DATA0/9.1A

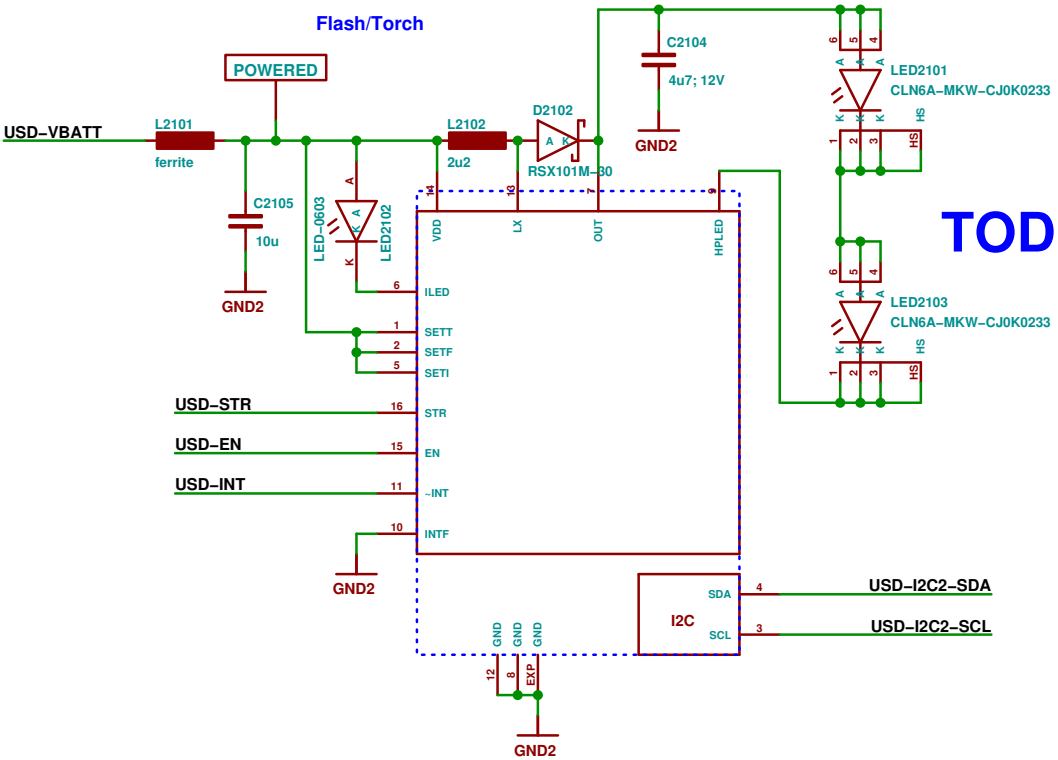
MMC3–DATA1/9.1A
MMC3–DATA2/9.1A
MMC3–DATA3/9.1A
GPIO–WLAN–IRQ/9.1A
GPIO–BT–EN/9.1C
UART1–RX/9.1C
UART1–RTS/9.1C
UART1–CTS/9.1D
UART1–TX/9.1D
MCBSP3–FCK/9.1D
MCBSP3–CLK/9.1D
MCBSP3–DR/9.1D
MCBSP3–DX/9.1D
SYSCLK/9.3C
32KHZ/9.4A
GPIO–FM–EN/9.3A
GPIO–FMIRQ/9.3A
MCBSP2–FCK/9.3A
MCBSP2–CLK/9.3A
MCBSP2–DR/9.3A
MCBSP2–DX/9.3A
GPIN115/10.3B
GPIO56/10.3A
GPIO$51/10.3B
GPIO$55/10.4A
GPIO$56/10.4A
ACCEL–INT/10.4C
N$129/11.2A
N$148/11.1A
N$149/11.1A
N$150/11.1A
N$153/11.1A
N$154/11.1A
GPIO–ECI1/13.3B
GPIO–ECI0/13.3C
ECI–ADC/13.3C
VMMC2/12.1A
GPIO–HP–EN/12.1B
GPIO$60/12.2D
GPIO177/12.4C
GPIO–HF–EN/14.1B
GPIO–FLASH–STR/15.1A
GPIO–FLASH–EN/15.1A
GPIO–FLASH–INT/15.1A
GPIO–BATT–LID/15.1B
SD–CMD/15.2A
SD–CLK/15.2A
SD–CD/15.2B
SD–VDD/15.2A
SD–DAT0/15.2B
SD–DAT1/15.2B
SD–DAT2/15.2A
SD–DAT3/15.2A
VIB+/15.1D
VIB–/15.1D
3V3/19.1D
2V5/13.3B
1V8/19.1D
VBUS/18.1C
OTG–D–/3.1B
OTG–D+/3.1B
OTG–ID/2.2B
VBUS–MODEM/6.3B
USB–WWAN–D+/18.3A
USB–WWAN–D–/18.3A
2V7/8.4C
GPIO–CAM–COVER/15.1B
N$38

Pin assignment musr be optimized for final component placement
we might have to switch to 80 or 100 pin connectors





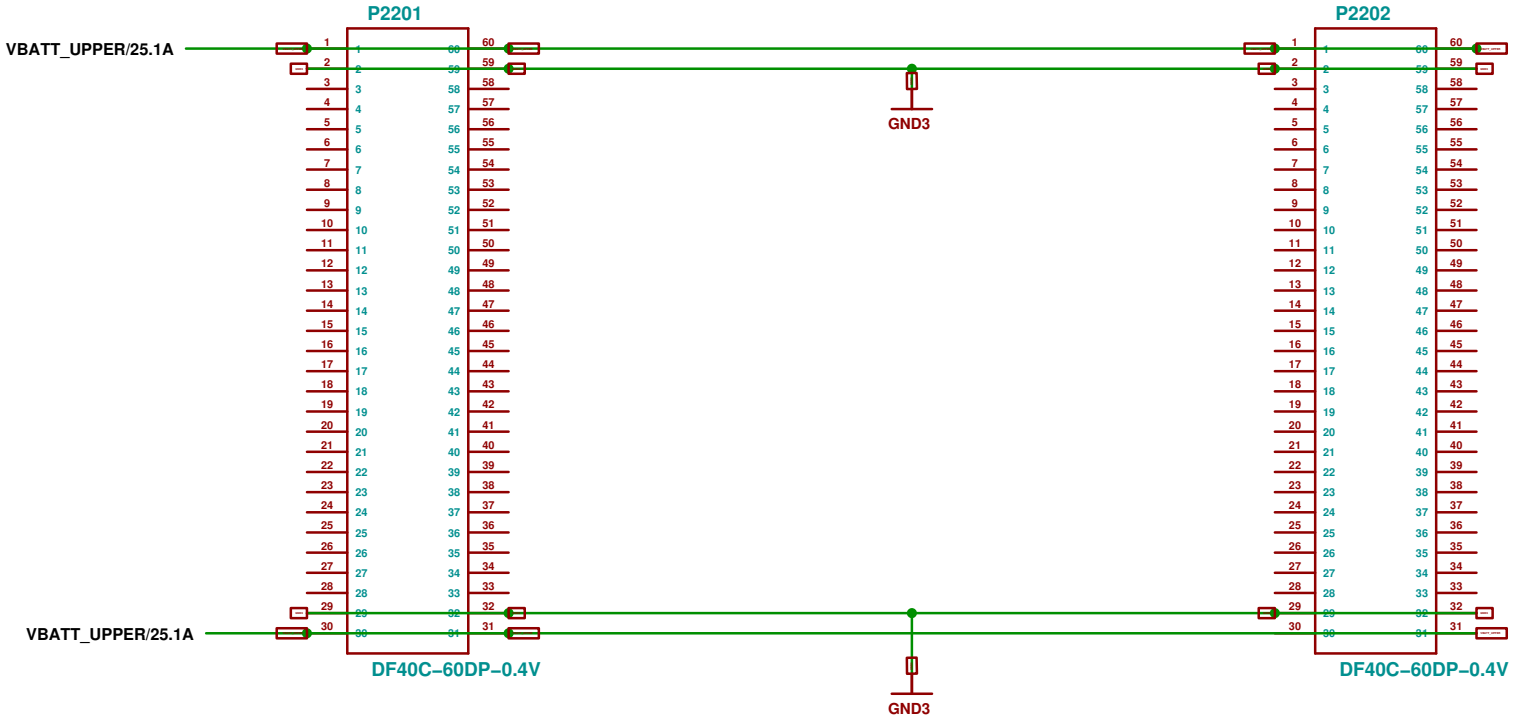
TODO: use TMD26713



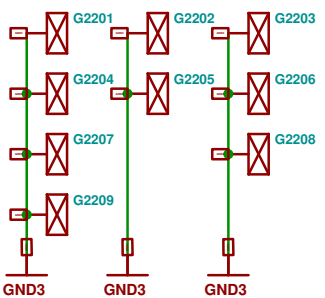
TODO: wrong LEDs

TODO: flash controller is now on LOWER, not BOB

to be adjusted to lower board connector

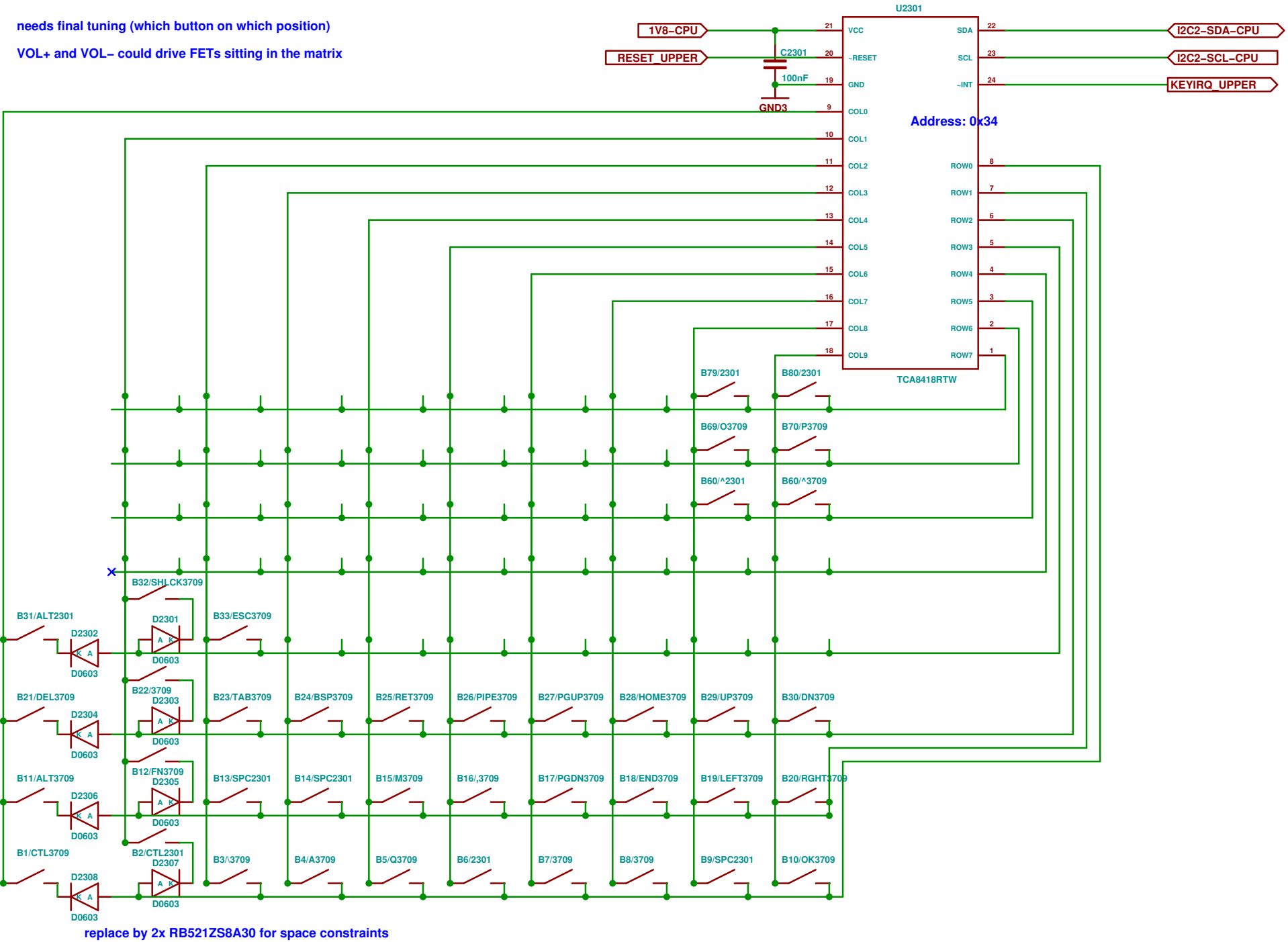


SHIELD



needs final tuning (which button on which position)

VOL+ and VOL– could drive FETs sitting in the matrix



replace by 2x RB521ZS8A30 for space constraints

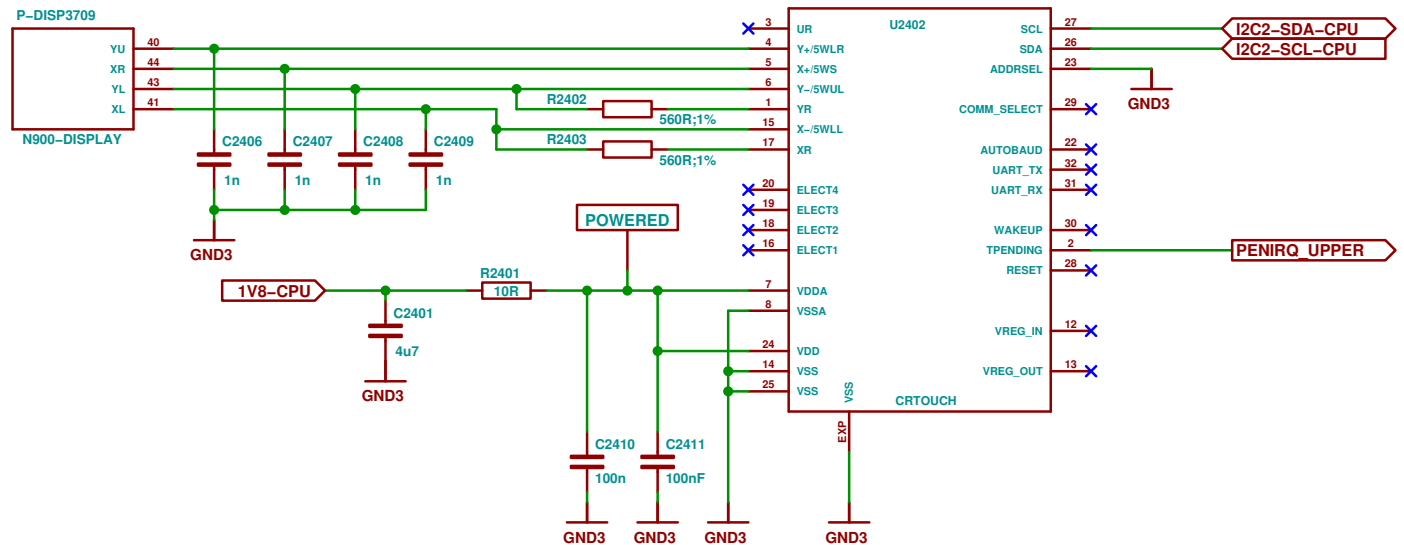
TODO: remove 3709 in comp ref

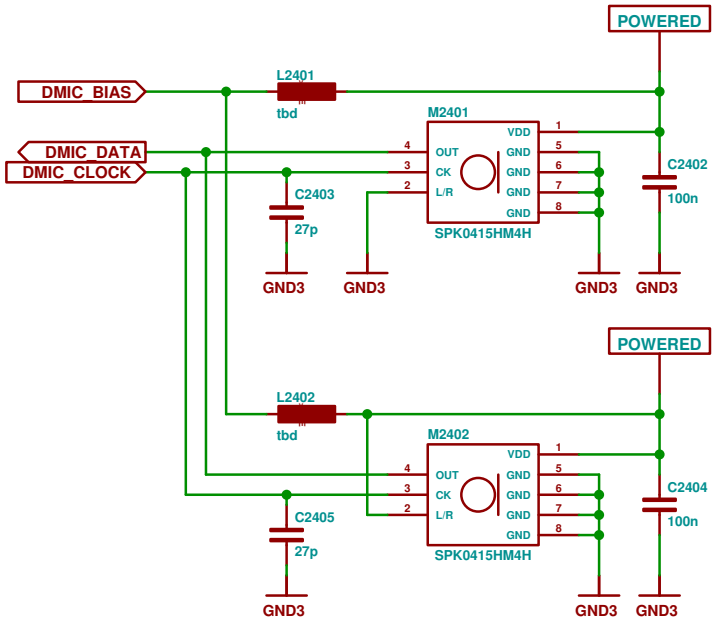
TODO: remove keycap from comp ref

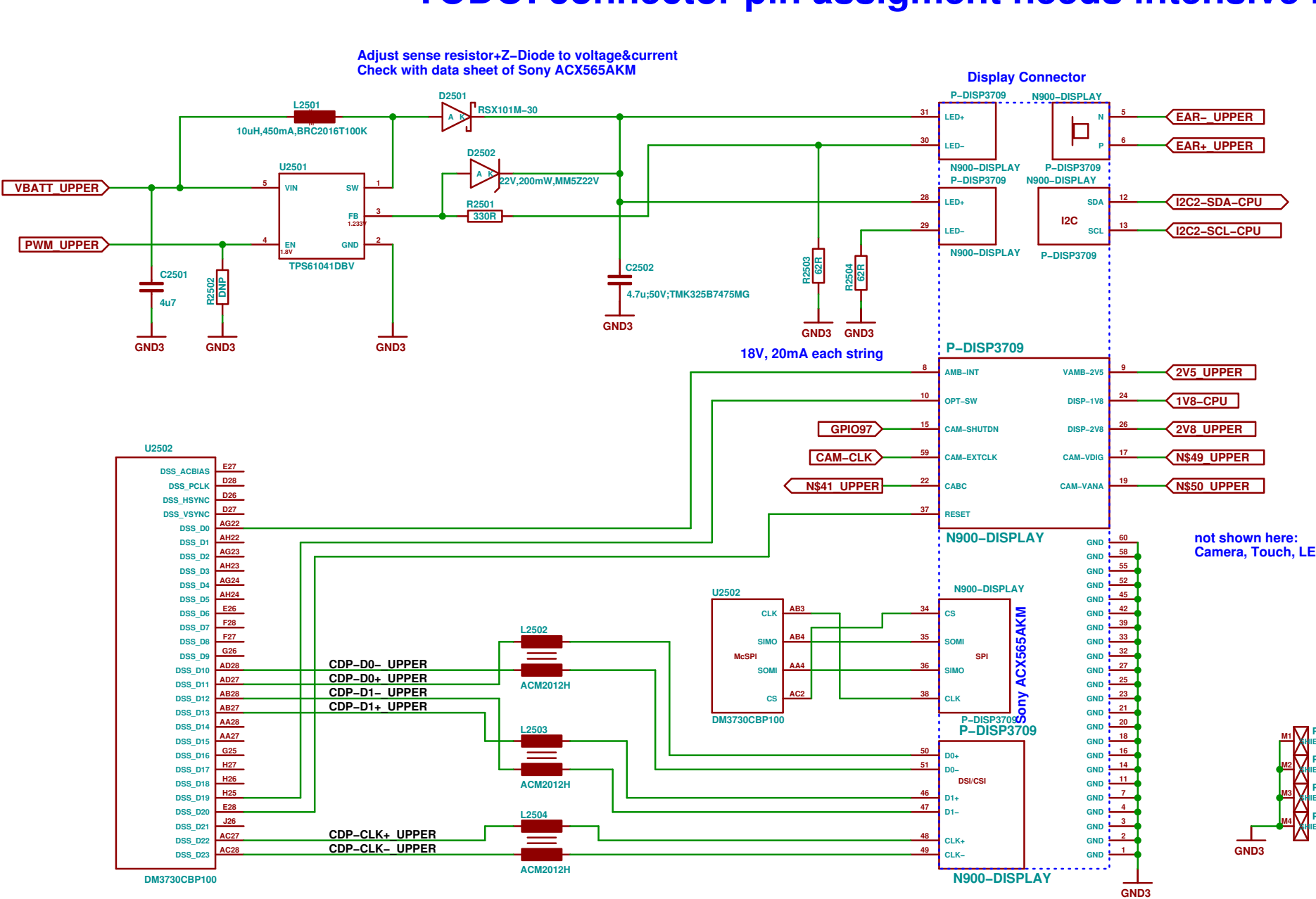
TODO: sort out 6 "ext" buttons

TODO: rearrange matrix to avoid diodes ?

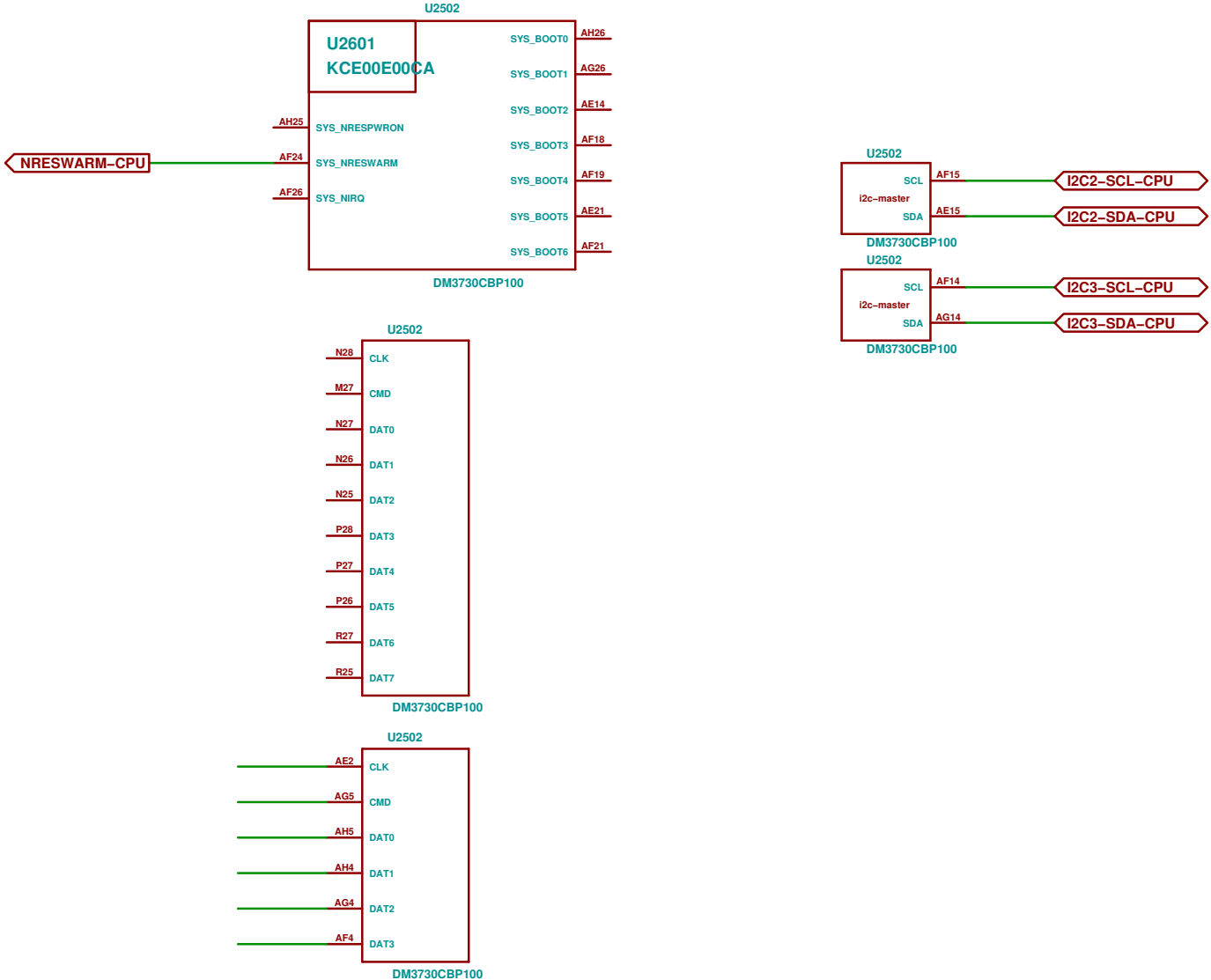
Resistive Touch (display connector)



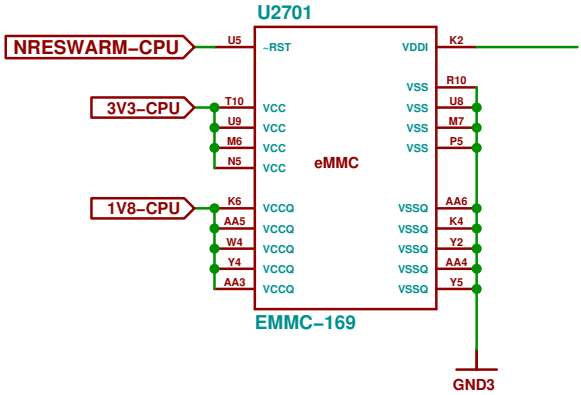


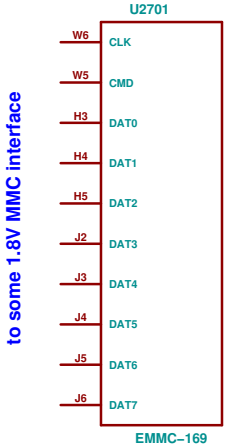

Adjust sense resistor+Z-Diode to voltage&current
Check with data sheet of Sony ACX565AKM
Display Connector
L2501
10uH,450mA,BRC2016T100K
D2501
RSX101M-30
D2502
22V,200mW,MM5Z22V
R2501
330R
U2501
VBATT_UPPER
PWM_UPPER
VIN
SW
FB
1.233V
EN
1.8V
GND
TPS61041DBV
C2501
4u7
R2502
DNP
C2502
4.7u;50V;TMK325B7475MG
R2503
62R
R2504
62R
GND3
P-DISP3709
N900-DISPLAY
LED+
LED-
N
P
EAR-_UPPER
EAR+_UPPER
I2C
SDA
SCL
I2C2-SDA-CPU
I2C2-SCL-CPU
18V, 20mA each string
AMB-INT
OPT-SW
CAM-SHUTDN
CAM-EXTCLK
CABC
RESET
VAMB-2V5
DISP-1V8
DISP-2V8
CAM-VDIG
CAM-VANA
GPIO97
CAM-CLK
N$41_UPPER
2V5_UPPER
1V8-CPU
2V8_UPPER
N$49_UPPER
N$50_UPPER
not shown here:
Camera, Touch, LE
U2502
DSS_ACBIAS
DSS_PCLK
DSS_HSYNC
DSS_VSYNC
DSS_D0
DSS_D1
DSS_D2
DSS_D3
DSS_D4
DSS_D5
DSS_D6
DSS_D7
DSS_D8
DSS_D9
DSS_D10
DSS_D11
DSS_D12
DSS_D13
DSS_D14
DSS_D15
DSS_D16
DSS_D17
DSS_D18
DSS_D19
DSS_D20
DSS_D21
DSS_D22
DSS_D23
DM3730CBP100
CDP-D0- UPPER
CDP-D0+ UPPER
CDP-D1- UPPER
CDP-D1+ UPPER
CDP-CLK+ UPPER
CDP-CLK- UPPER
L2502
L2503
L2504
ACM2012H
CLK
SIMO
McSPI
SOMI
CS
SPI
Sony ACX565AKM
D0+
D0-
DSI/CSI
D1+
D1-
CLK+
CLK-
GND

INCOMPLETE in V2



INCOMPLETE in V2





to some 1.8V MMC interface

INCOMPLETE in V2

R2801
(0R)

VSYS_UPPER

U2801
LTC3355

should drive TPS65950

VBAT(->TPS65950)_UPPER

C2801
tbd

GND3

U2803

C8 IO.1P8
H4 ADCIN0
J3 ADCIN1
G3 ADCIN2
J9 STARTADC
N16 VREF
N15 AGND
A2 RFID.EN
GPIO13/LEDSYNC G11
LEDA/VIBRA.P F15
LEDB/VIBRA.M G15
LEDGND F16
NC B14
MSECURE H8

TPS65950

U2802

A2 REFCLK
A3 STP
A4 DIR
B5 NXT
B4 DATA0
C5 DATA1
C4 DATA2
D5 DATA3
D4 DATA4
E5 DATA5
E4 DATA6
D3 DATA7
B2 RESETB
A5 CLKOUT
VBAT C1
VBUS C2
DM D1
DP E1
ID B1
SPK_L E3
SPK_R E2
VDD3.3 D2
VDD1.8 B3
RBIAS A1
GND C3

this goes through B2B to modem

VBUS-MODEM-CPU
MODEM-CPU-D-
MODEM-CPU-D+

needs a small charge pump to gener

USB3322

U2803

L15 UCLK
L14 STP
L13 DIR
M13 NXT
K14 DATA0/TX
K13 DATA1/RX
J14 DATA2/RTSI
J13 DATA3/CTSO
G14 DATA4
G13 DATA5
F14 DATA6
F13 DATA7
VBUS R8
DN/UART3.TXD T11
DP/UART3.RXD T10
ID R11

this goes through B2B to OTG socket

VBUS-CPU
OTG-CPU-D-
OTG-CPU-D+
OTG-CPU-ID

TPS65950

U2803

VAC N5
PCHGAC N4
PCHGUSB N6
ICTLAC1 N7
ICTLAC2 P2
ICTLUSB1 P6
ICTLUSB2 P1
VPRECH N2
VCCS P5
VBATS P4
N1 BCIAUTO
VBAT R5

TPS65950

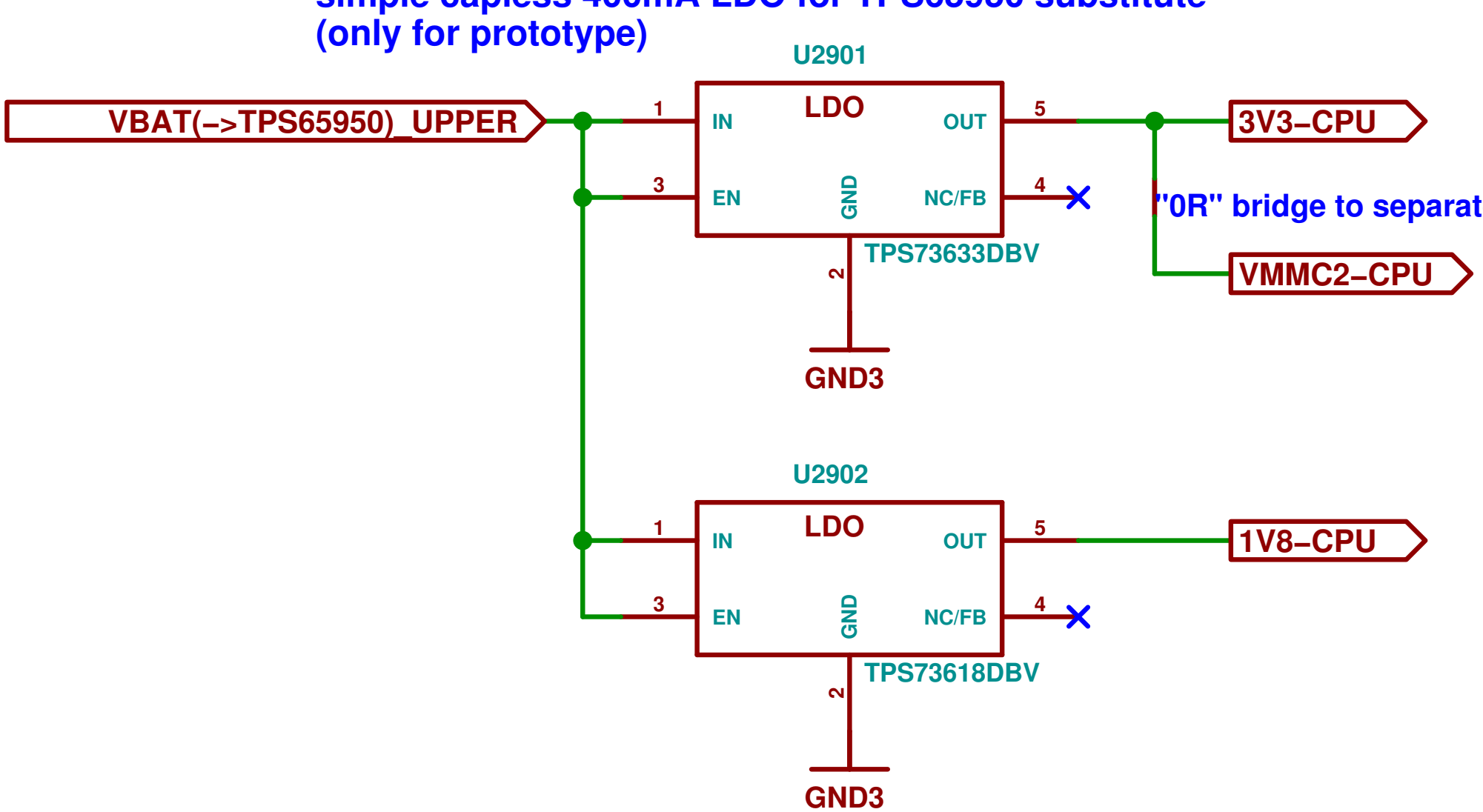
U2803

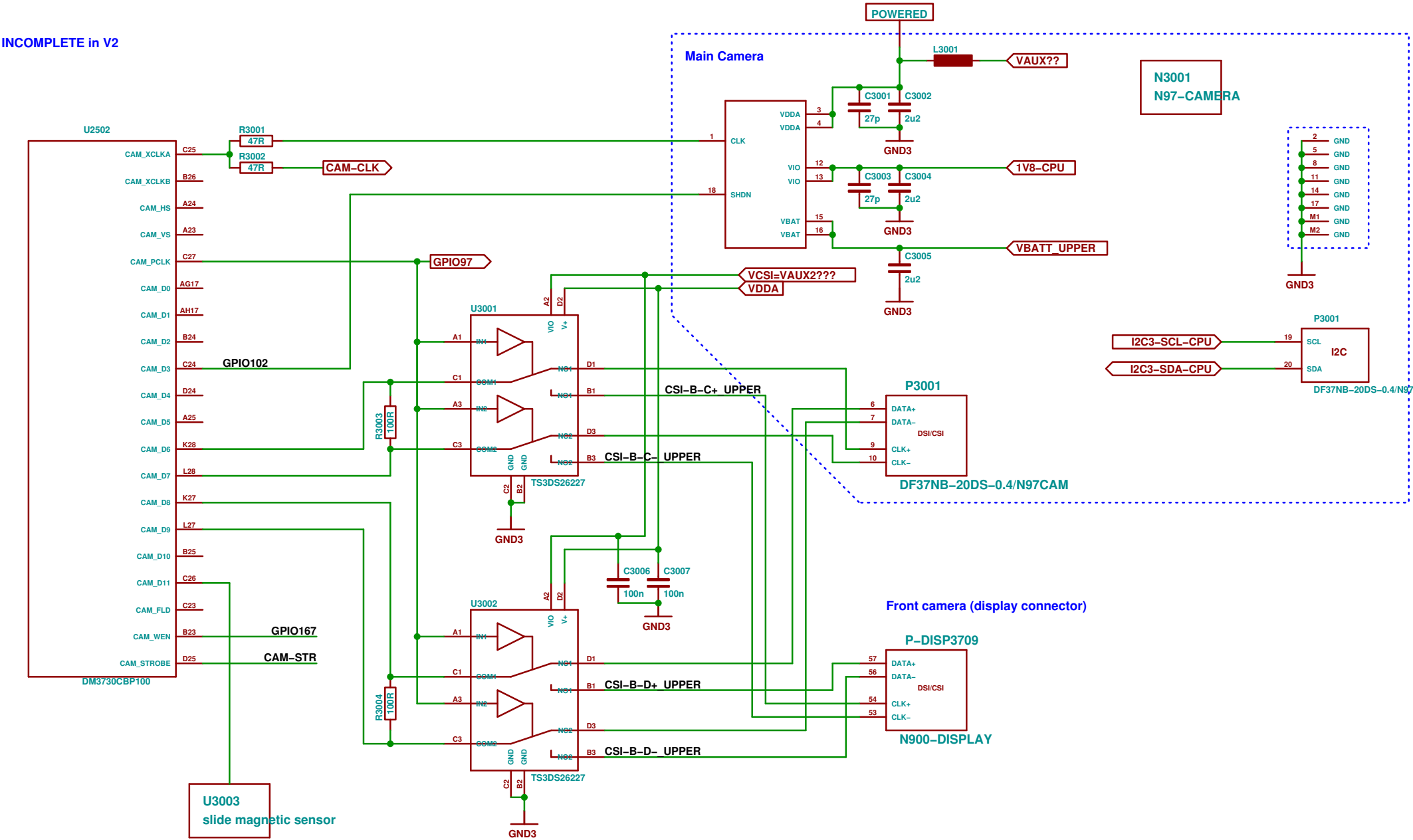
P16 32KXIN
P15 32KXOUT
A14 HFCLKIN
C6 CLKEN
D7 CLKEN2
32KCLKOUT N10
HFCLKOUT R12
CLKREQ G10
CLK256FS D13
BKBAT M14

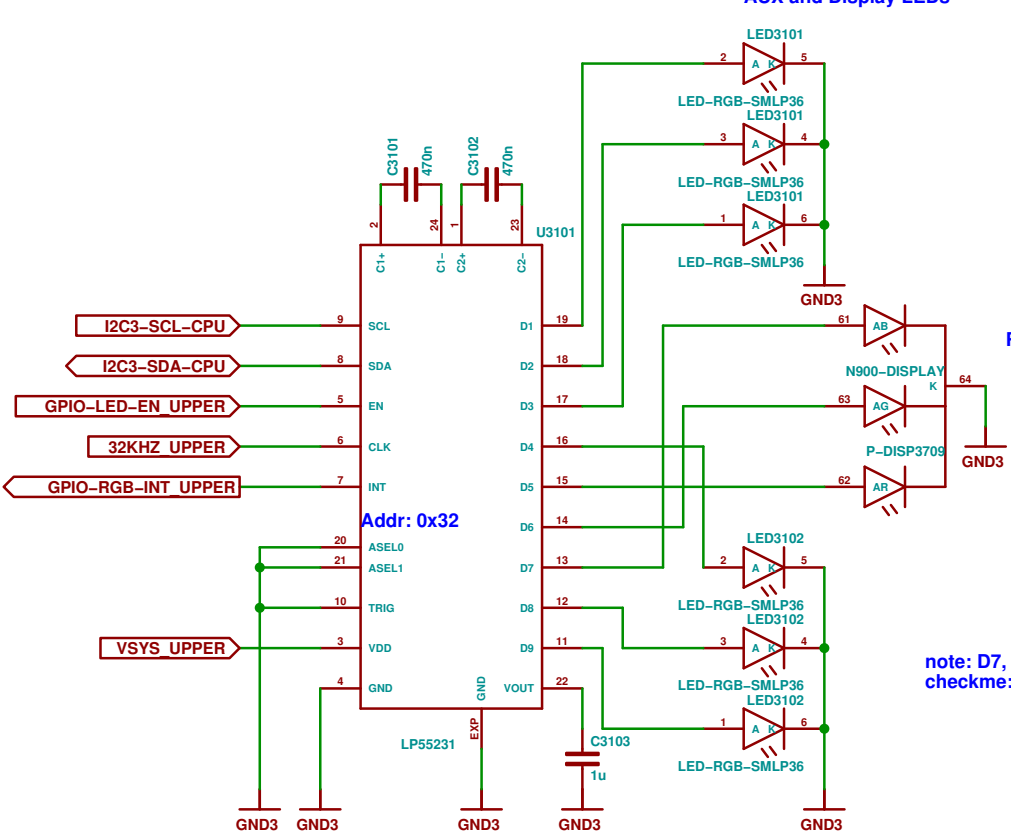
TPS65950

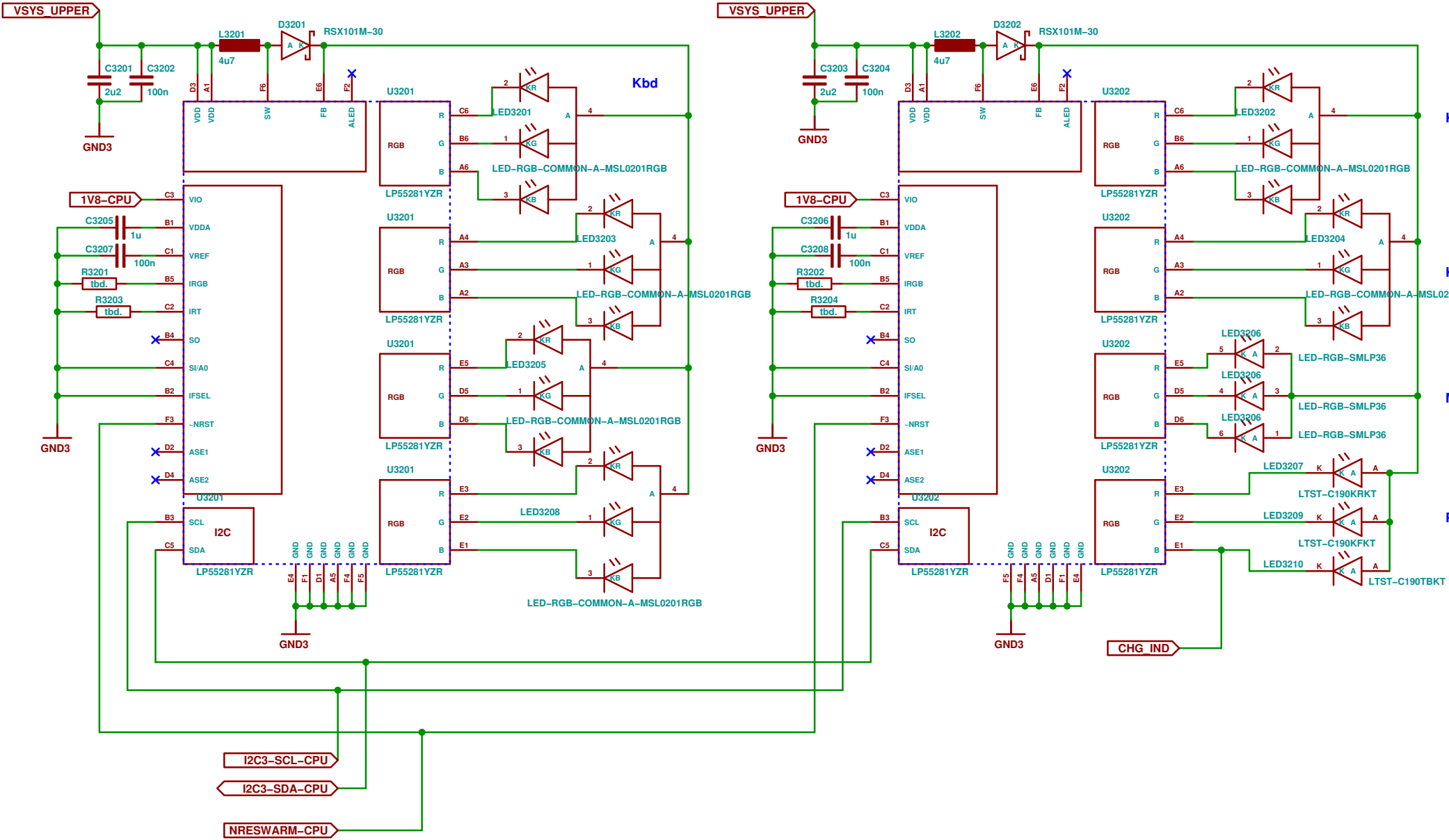
C2802
PAS3225P3R3113

GND3


Simple capless 400mA LDO for TPS65950 substitute
(only for prototype)
U2901
LDO
VBAT(–>TPS65950)_UPPER
1
IN
OUT
5
3V3–CPU
3
EN
GND
NC/FB
4
"0R" bridge to separat
TPS73633DBV
2
VMMC2–CPU
GND3
U2902
LDO
1
IN
OUT
5
1V8–CPU
3
EN
GND
NC/FB
4
TPS73618DBV
2
GND3


INCOMPLETE in V2
Main Camera
POWERED
L3001
VAUX??
N3001
N97-CAMERA
U2502
R3001
47R
R3002
47R
CAM-CLK
CAM_XCLKA
CAM_XCLKB
CAM_HS
CAM_VS
CAM_PCLK
CAM_D0
CAM_D1
CAM_D2
CAM_D3
CAM_D4
CAM_D5
CAM_D6
CAM_D7
CAM_D8
CAM_D9
CAM_D10
CAM_D11
CAM_FLD
CAM_WEN
CAM_STROBE
DM3730CBP100
GPIO102
GPIO97
GPIO167
CAM-STR
C3001
C3002
27p
2u2
GND3
VDDA
VDDA
CLK
SHDN
VIO
VIO
VBAT
VBAT
1V8-CPU
C3003
C3004
VBATT_UPPER
C3005
VCSI=VAUX2???
VDDA
U3001
TS3DS26227
R3003
100R
R3004
100R
C3006
C3007
100n
U3002
CSI-B-C+_UPPER
CSI-B-C-_UPPER
CSI-B-D+_UPPER
CSI-B-D-_UPPER
P3001
DATA+
DATA-
DSI/CSI
CLK+
CLK-
DF37NB-20DS-0.4/N97CAM
Front camera (display connector)
P-DISP3709
N900-DISPLAY
U3003
slide magnetic sensor
I2C3-SCL-CPU
I2C3-SDA-CPU
SCL
SDA
I2C
DF37NB-20DS-0.4/N9
GND


AUX and Display LEDs
LED3101
LED-RGB-SMLP36
LED3101
LED-RGB-SMLP36
LED3101
LED-RGB-SMLP36
GND3
C3101
470n
C3102
470n
U3101
C1+
C1-
C2+
C2-
I2C3-SCL-CPU
I2C3-SDA-CPU
GPIO-LED-EN_UPPER
32KHZ_UPPER
GPIO-RGB-INT_UPPER
SCL
SDA
EN
CLK
INT
D1
D2
D3
D4
D5
D6
D7
D8
D9
VOUT
GND
EXP
Addr: 0x32
ASEL0
ASEL1
TRIG
VDD
VSYS_UPPER
LP55231
C3103
1u
N900-DISPLAY
P-DISP3709
AB
AG
AR
K
LED3102
LED-RGB-SMLP36
LED3102
LED-RGB-SMLP36
LED3102
LED-RGB-SMLP36
note: D7,
checkme:
GND3
GND3
GND3
GND3
GND3


VSYS_UPPER
L3201
4u7
D3201
RSX101M-30
C3201
2u2
C3202
100n
GND3
Kbd
U3201
LP55281YZR
LED3201
LED-RGB-COMMON-A-MSL0201RGB
1V8-CPU
C3205
1u
C3207
100n
R3201
tbd.
R3203
tbd.
VIO
VDDA
VREF
IRGB
IRT
SO
SI/A0
IFSEL
~NRST
ASE1
ASE2
I2C
SCL
SDA
LED3203
LED3205
LED3208
VSYS_UPPER
L3202
4u7
D3202
RSX101M-30
C3203
2u2
C3204
100n
GND3
U3202
LP55281YZR
C3206
1u
C3208
100n
R3202
tbd.
R3204
tbd.
LED3202
LED3204
LED3206
LED-RGB-SMLP36
LED3207
LED3209
LED3210
LTST-C190KRKT
LTST-C190KFKT
LTST-C190TBKT
CHG_IND
I2C3-SCL-CPU
I2C3-SDA-CPU
NRESWARM-CPU

These connectors allow to "emulate" the DM3730 by connecting a BB-xM

INCOMPLETE
prototype only

connect to respective CPU-pads

P2301

Connect to OMAP3 McSPI1, I2C2, MMC2 / some GPIOs

VSYS_UPPER

GND3

I2C2-SDA-CPU

I2C2-SCL-CPU

NRESWARM-CPU

P2302

GND3

I2C3-SCL-CPU

I2C3-SDA-CPU

Connect to OMAP3 DSS

DSS / GPIOs, I2C3

P2303

Connect to OMAP3 Camera

VAUX4

VAUX3

GND3

connect to BB
by some Micro-USB cable

P-MODEM3709-OTG2

GND

5/GN

GND3

ID

4/ID

D+

3/D+

MODEM-CPU-D+

D-

2/D-

MODEM-CPU-D-

VB

1/VB

VBUS-MODEM-CPU

R3301 (0R)

VBUS-CPU

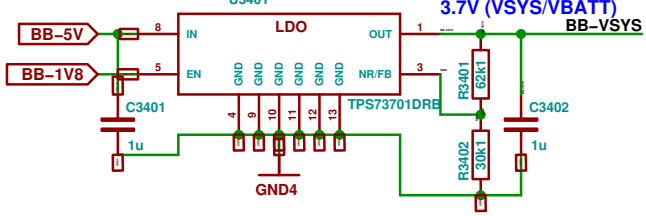
R3302 (0R)

OTG-CPU-D-

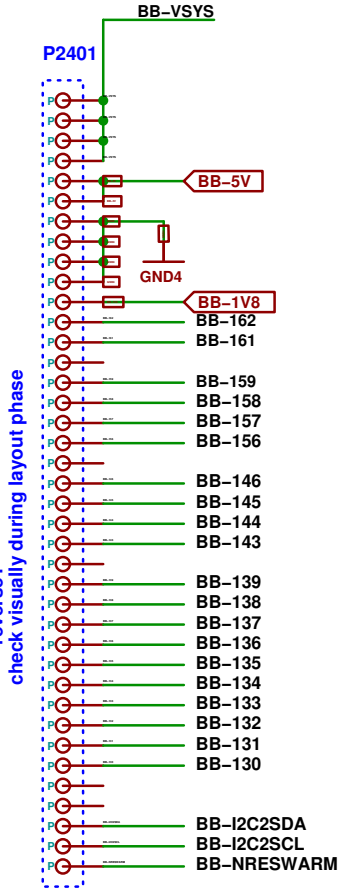
R3303 (0R)

OTG-CPU-D+

TODO: VBUS-MODEM ?

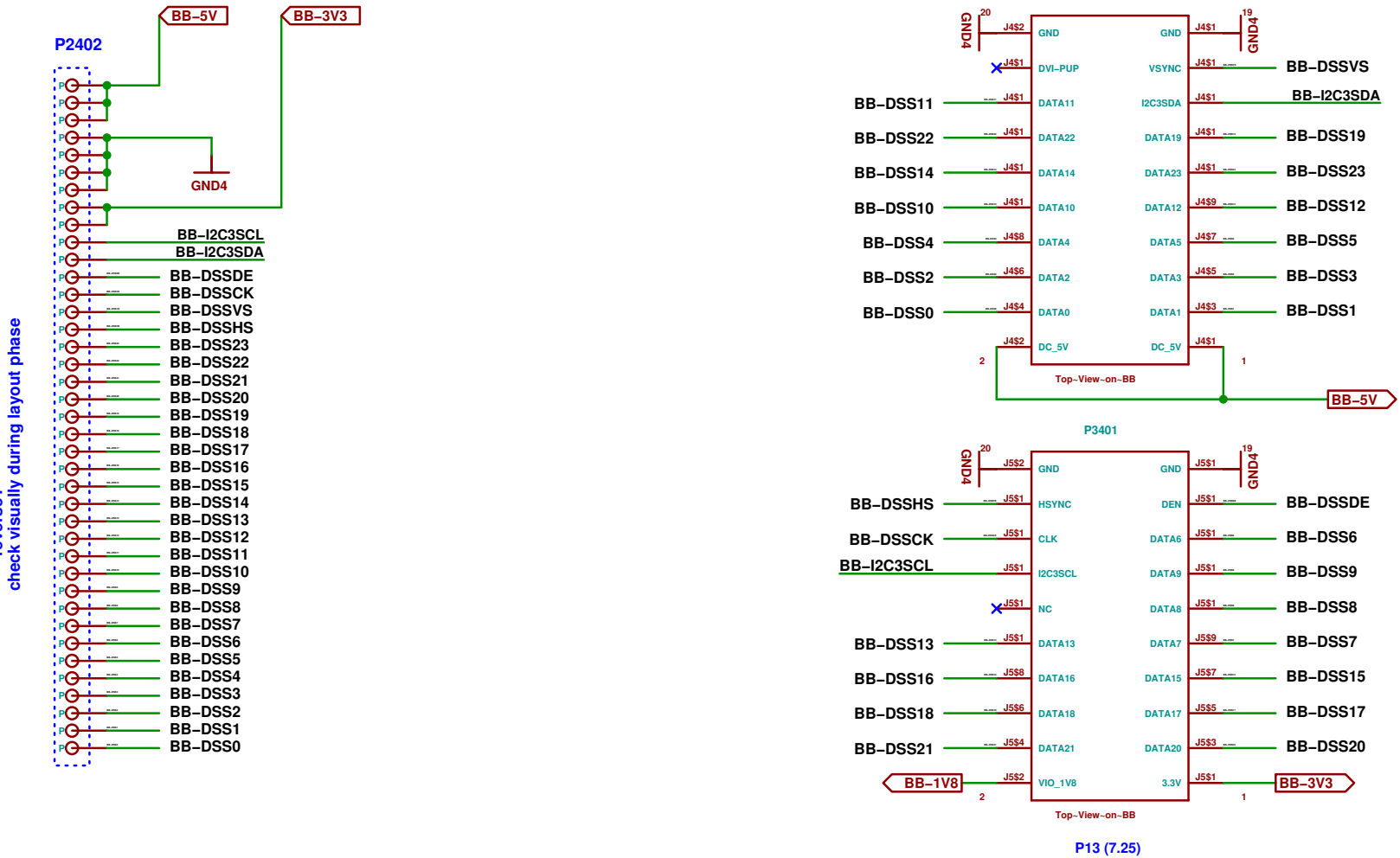


Ersetzen durch 2A buck converter

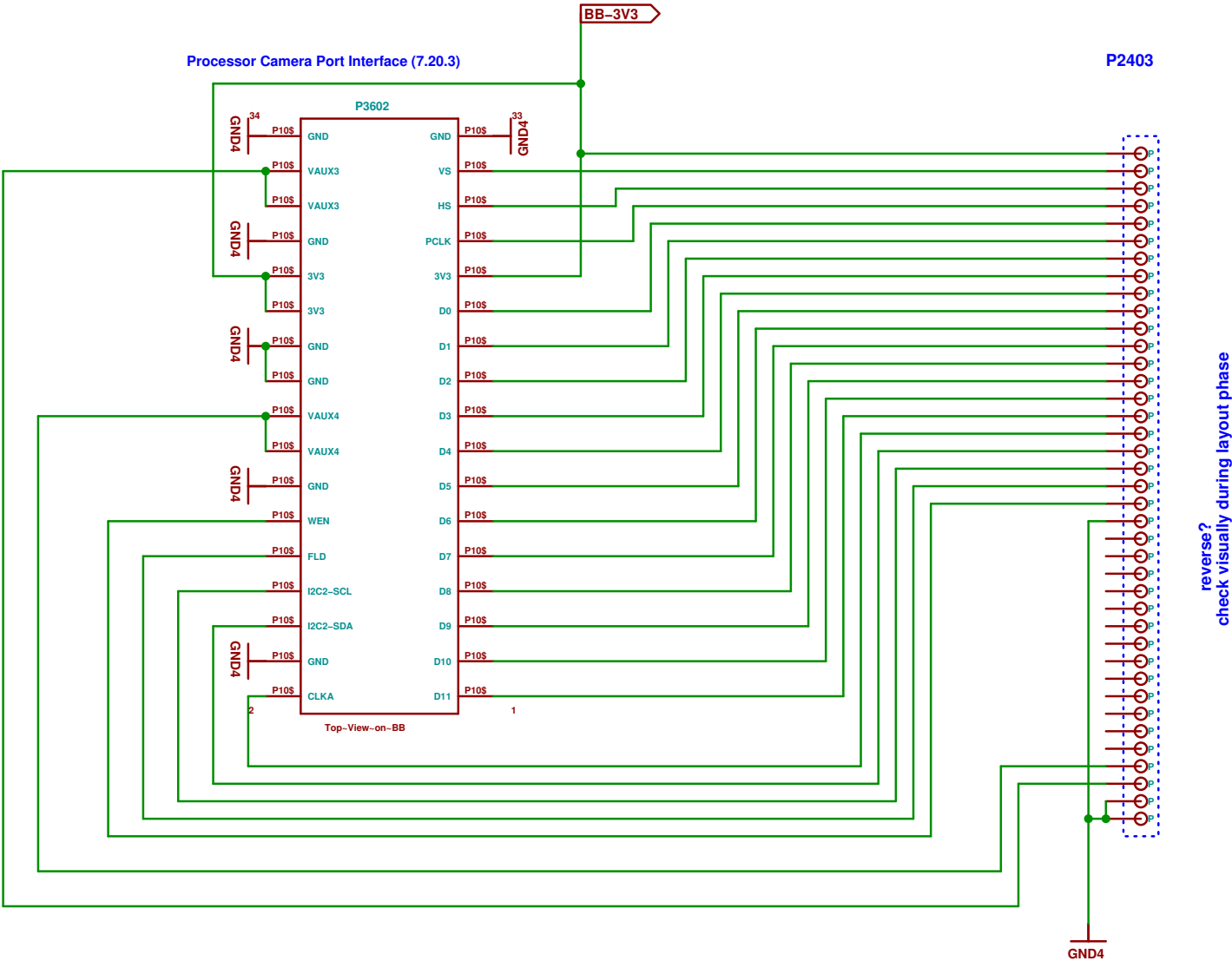


BB-xM Main Expansion Header (7.24)

TODO: needs decision on where to take this



TODO: needs decision on where to take this


BB-3V3
Processor Camera Port Interface (7.20.3)
P2403
P3602
34
33
GND4
P10$
GND
VAUX3
VAUX4
3V3
WEN
FLD
I2C2-SCL
I2C2-SDA
CLKA
VS
HS
PCLK
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
2
1
Top-View-on-BB
reverse?
check visually during layout phase

M6.5x Jumper cables to connect BB "XM" Adapter to Sppwr board

N3701
15015-0439

CPU

N3702
15015-0439

DISP

N3703
15015-0439

CAM

N3704
N900 case assembly

N3705
N97-CAMERA-HOLE

N3706
headset jac

N3707
STENCIL-TOP

N3708
STENCIL-BOTTOM

M6.5x Jumper cables to connect BB "XM" Adapter to Sppwr board

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