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CPU + PoP RAM/NAND

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Connector to BB-XM

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BB-XM Adapter (CPU)

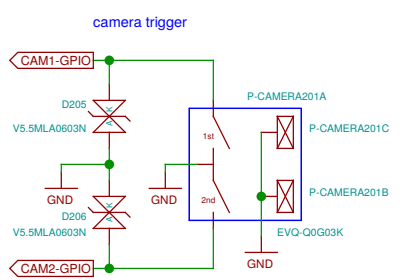
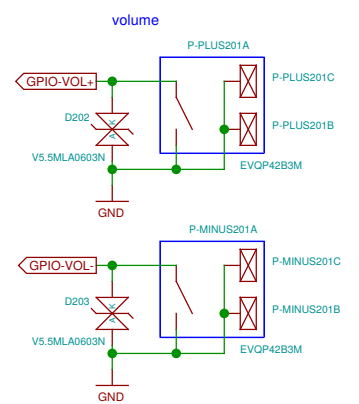
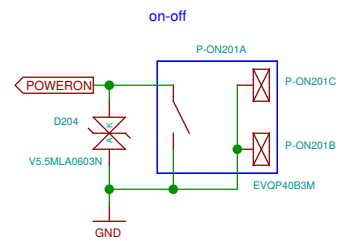
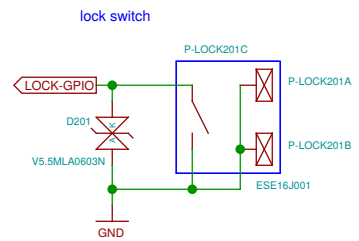
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BB-XM Adapter (DISP)

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BB-XM Adapter (CAM)

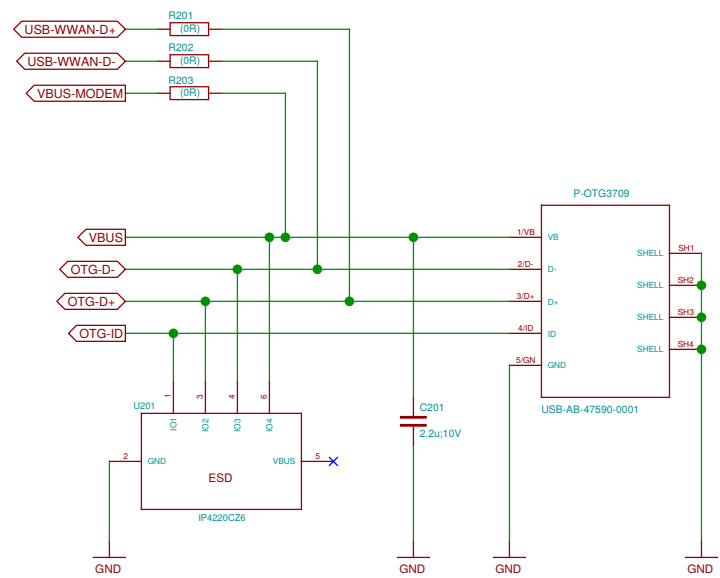
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No-Solder Components

Note regarding I2C addresses:
Addresses in the schematics are provided for convenience.
The authoritative source is
<https://neo900.org/git?p=misc;a=tree;f=i2c>

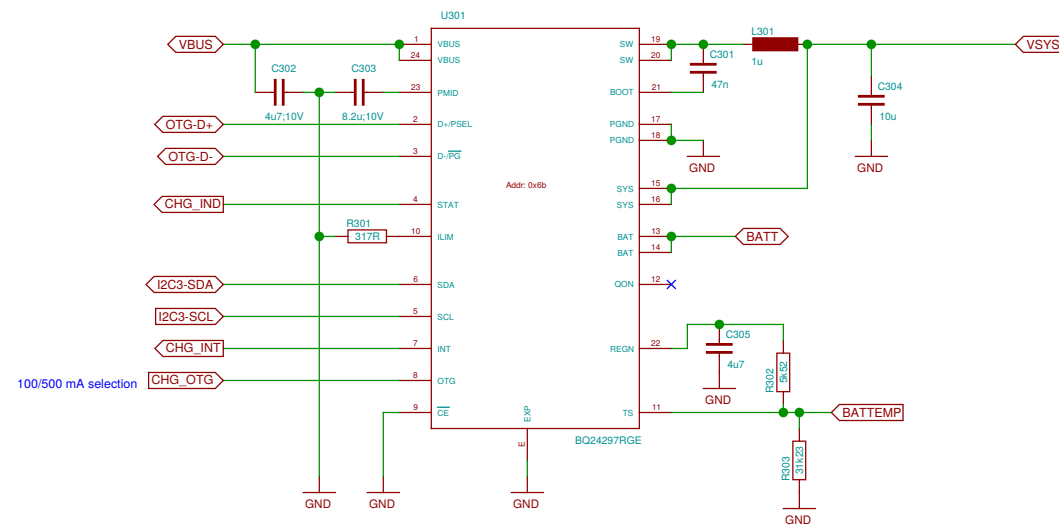
Sheet: /		
File: neo900.sch		
Title: Neo900		
Size: A3	Date: 16 JUL 2016	Rev:
%K		Id: 1/37



can be used to test/operate the modem through the OTG port (w/o UPPER PCB)

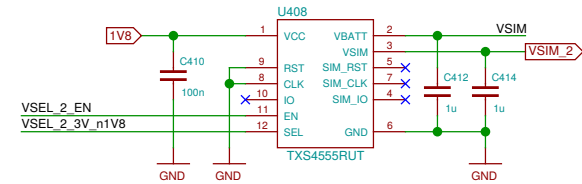
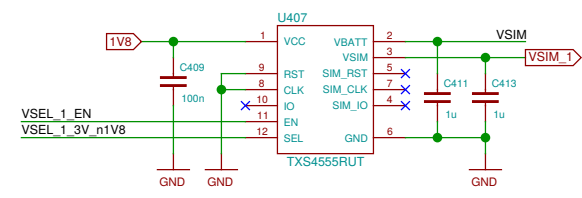
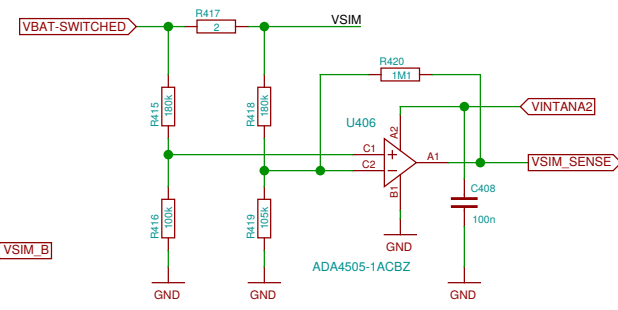
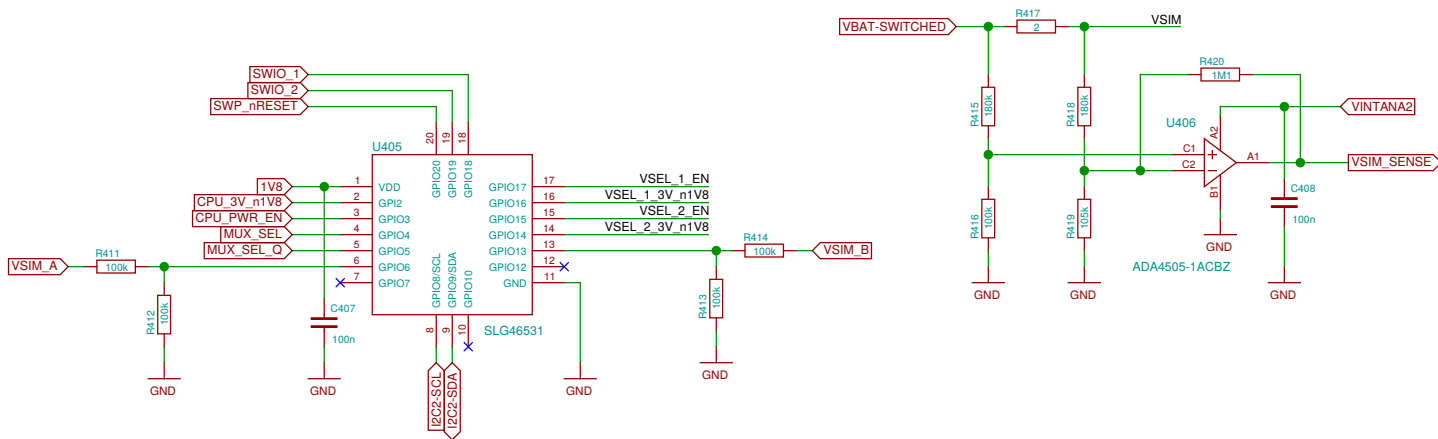
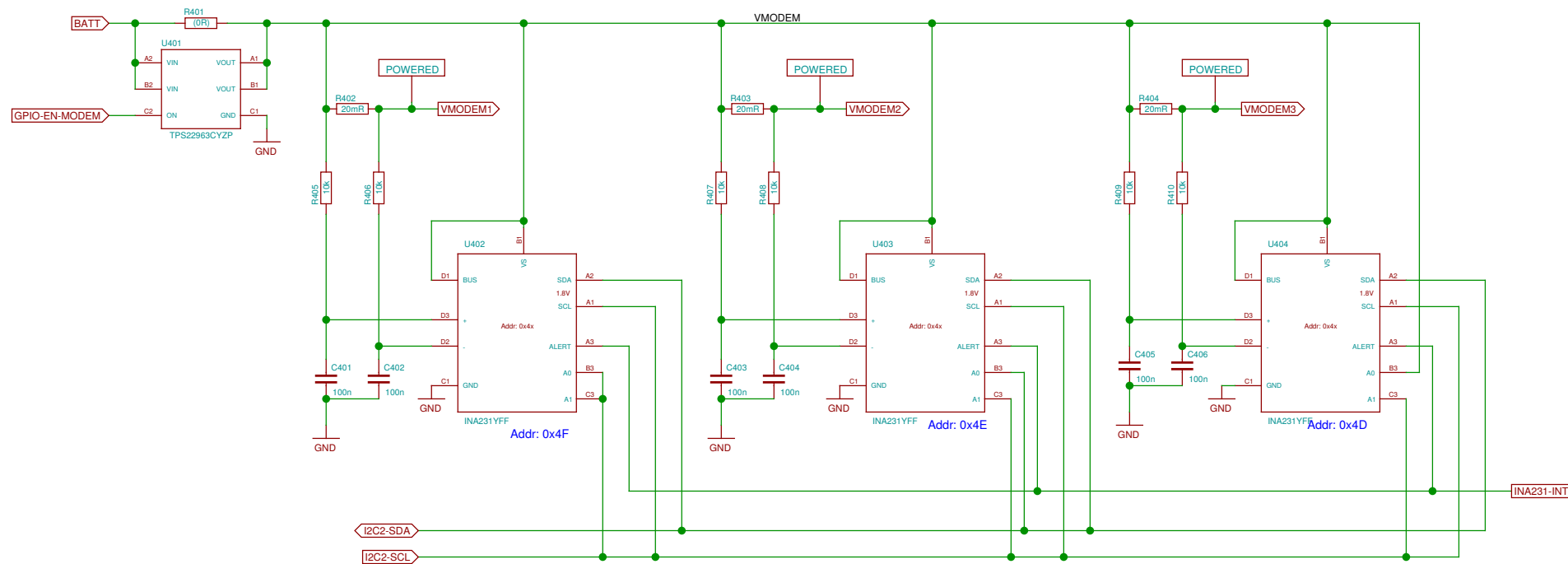


place in scan matrix? would need 3-4 wires to UPPER board instead of 2
 in any case it is sufficient to connect GPIO-VOL+ and VOL- to two pins on the B2B connector

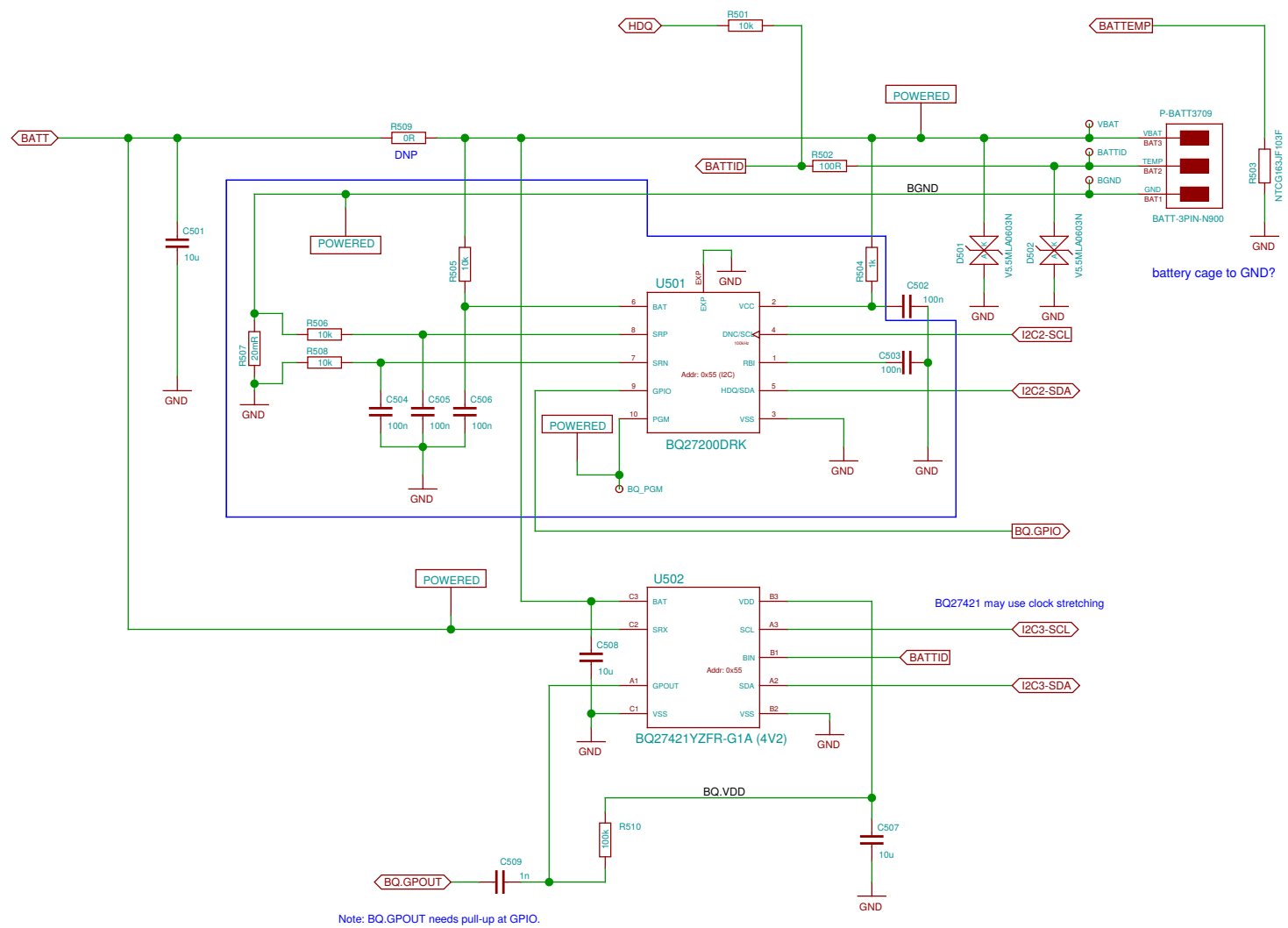


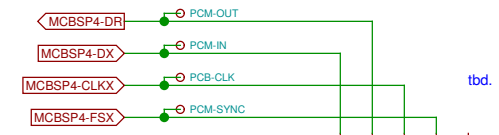
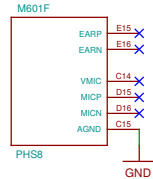
100/500 mA selection

Sheet: /Charger/OTG-Booster/		
File: neo900_SS_3.sch		
Title: Charger/OTG-Booster		
Size: A3	Date: 17 JUL 2016	Rev:
%K		Id: 3/37

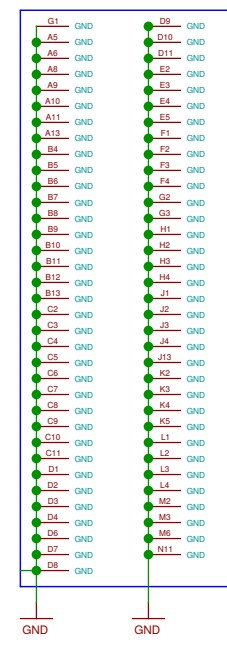
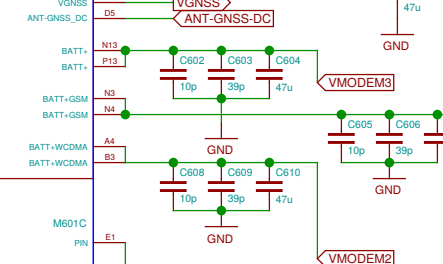
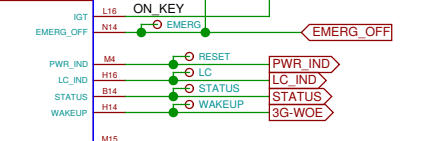
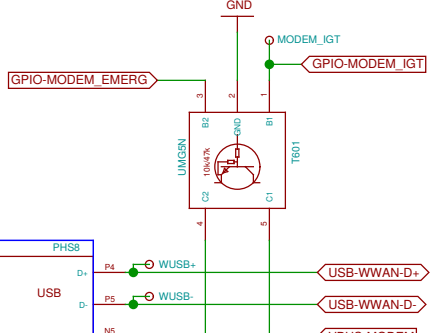
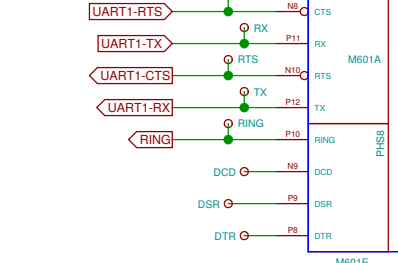
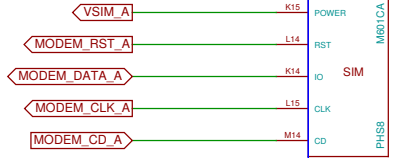


TODO: update SLG design for changed pins





tbd.



TODO: shield connection near D8

TODO: B-SIM bus FFS

Can we connect UART in parallel to Bluetooth UART (i.e. if BT is disabled we can unbrick the Modem?)

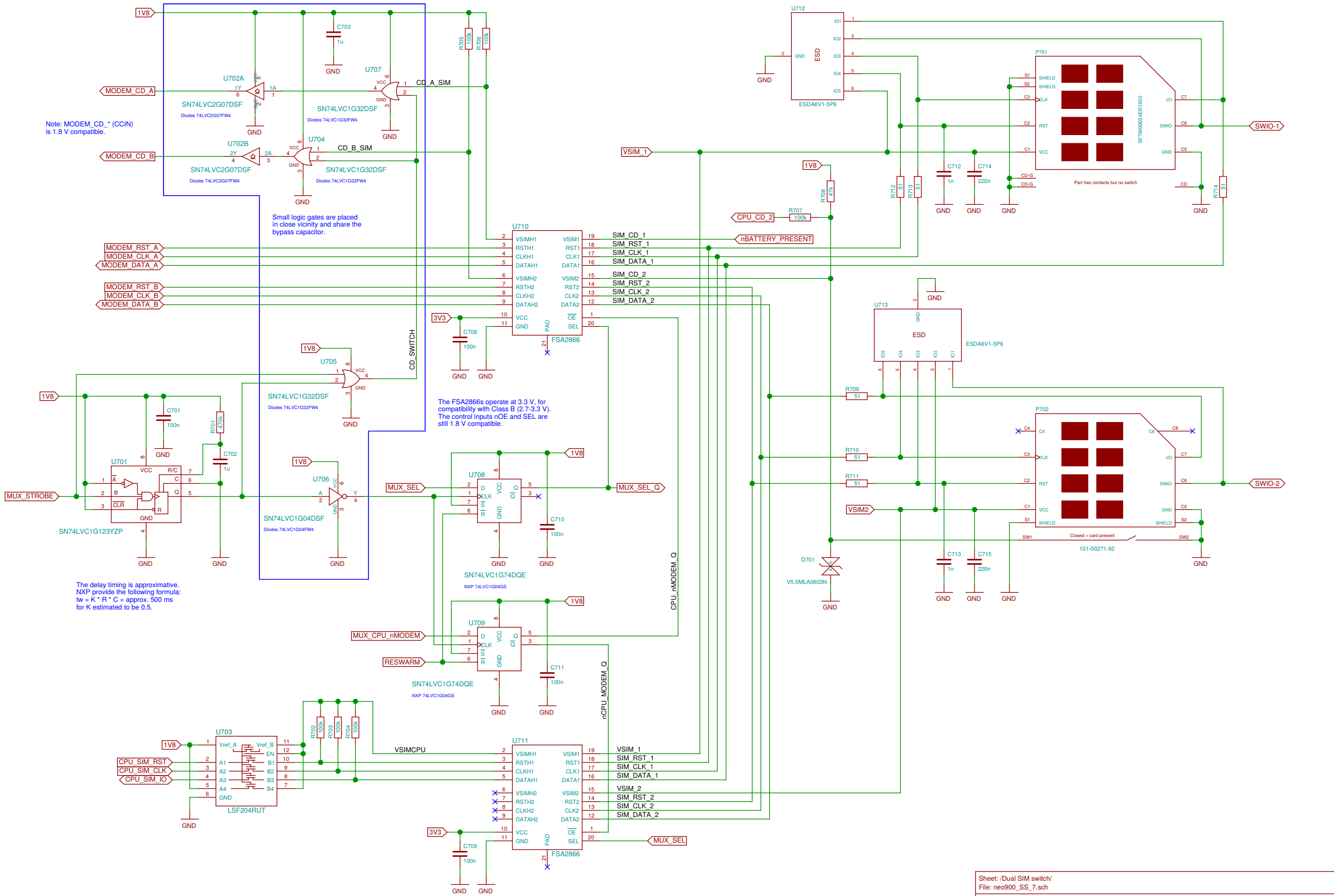
Sheet: /3G/4G Modem + SIM		File: neo900_SS_6.sch	
Title: 3G/4G Modem + SIM			
Size: A3	Date: 17 JUL 2016	Rev:	
%K		Id: 6/37	

Note: MODEM_CD_* (CCIN) is 1.8 V compatible.

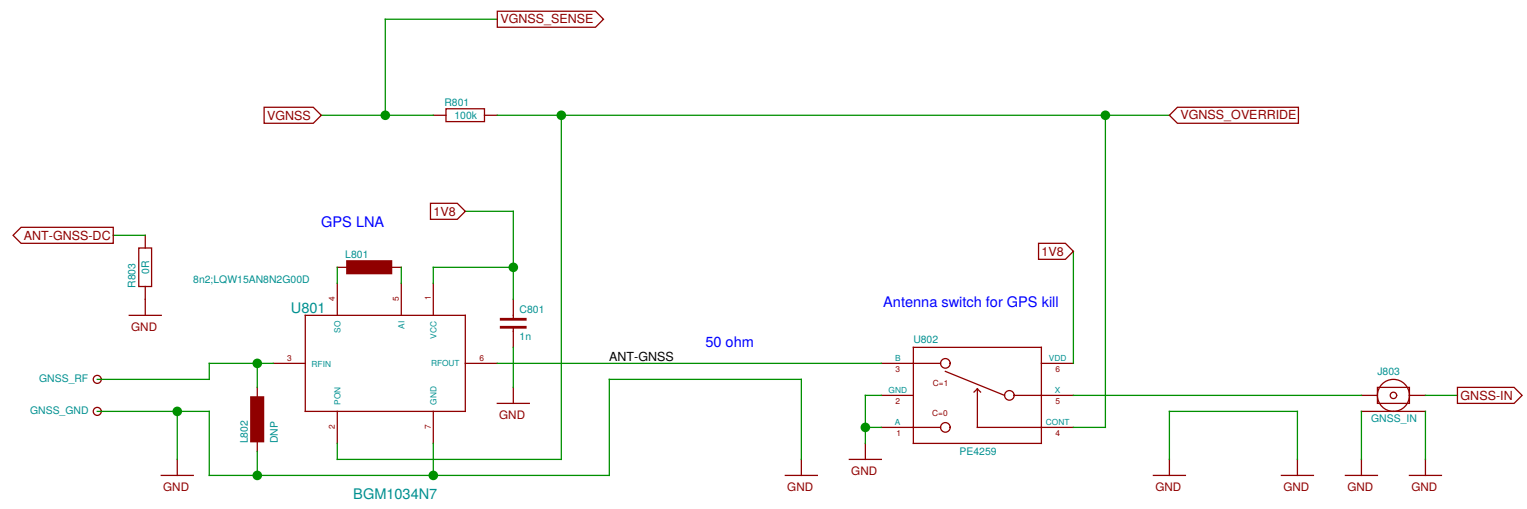
Small logic gates are placed in close vicinity and share the bypass capacitor.

The FSA2866s operate at 3.3 V, for compatibility with Class B (2.7-3.3 V). The control inputs nOE and SEL are still 1.8 V compatible.

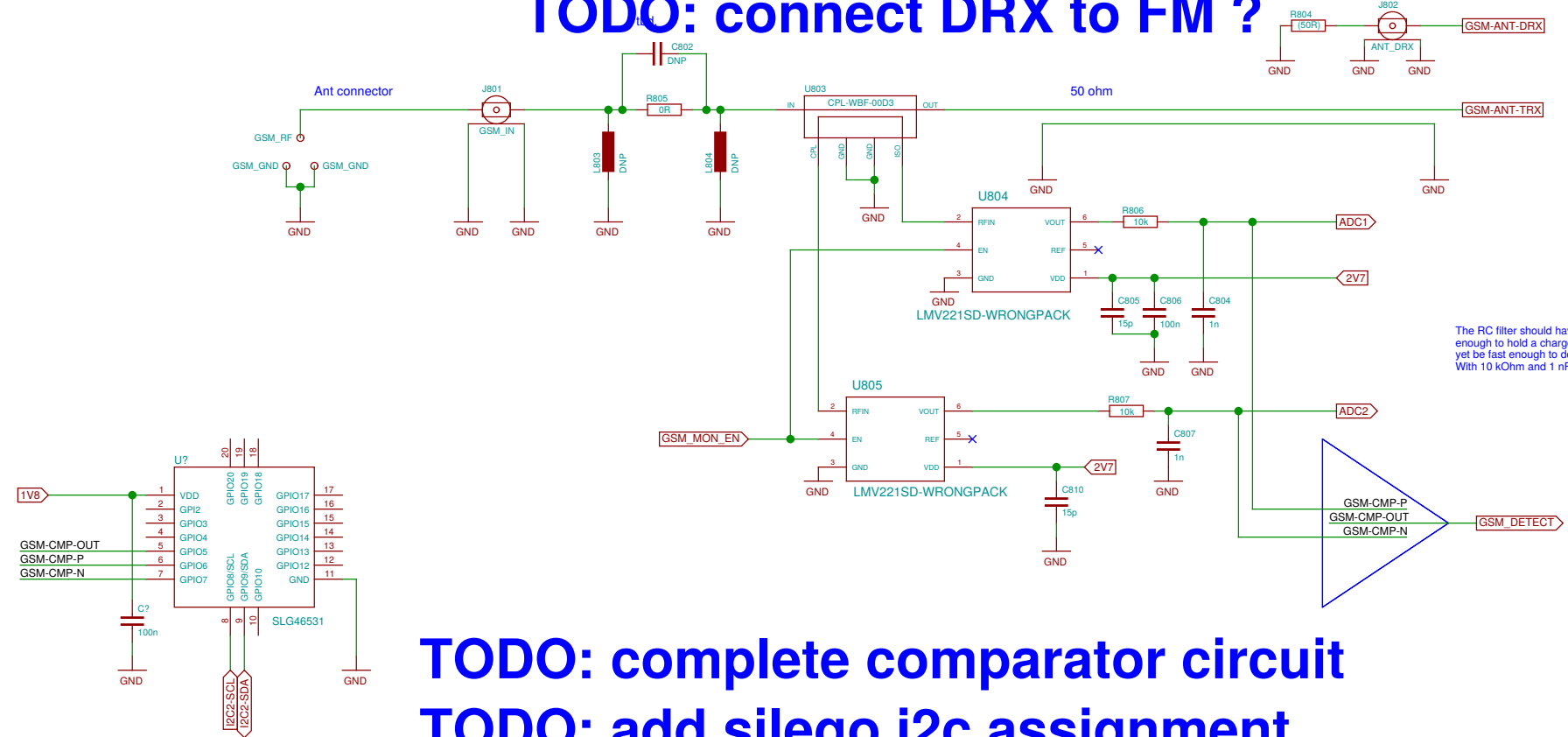
The delay timing is approximative. NXP provide the following formula: $t_w = K * R * C = \text{approx. } 500 \text{ ms}$ for K estimated to be 0.5.



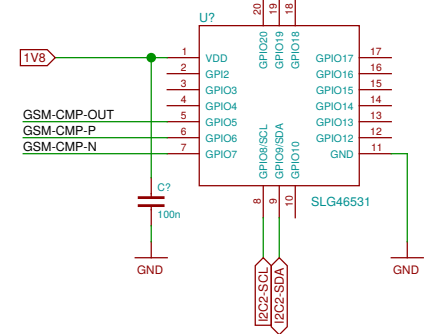
Sheet: /Dual SIM switch/ File: neo900_SS_7.sch		Title: Dual SIM switch	
Size: A3	Date: 17 JUL 2016	Rev: 7/37	
%K		Id: 7/37	



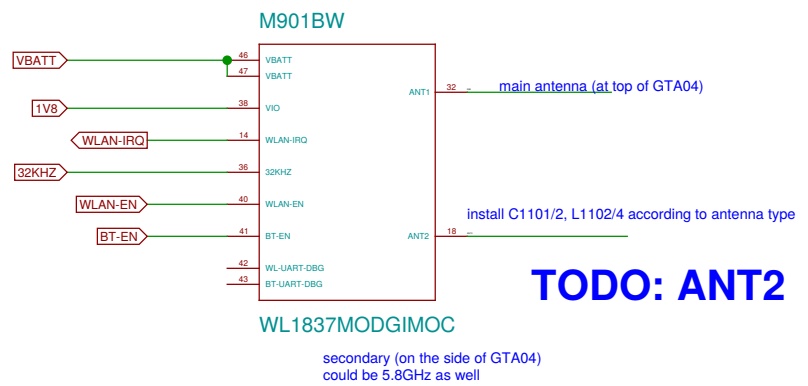
TODO: connect DRX to FM ?



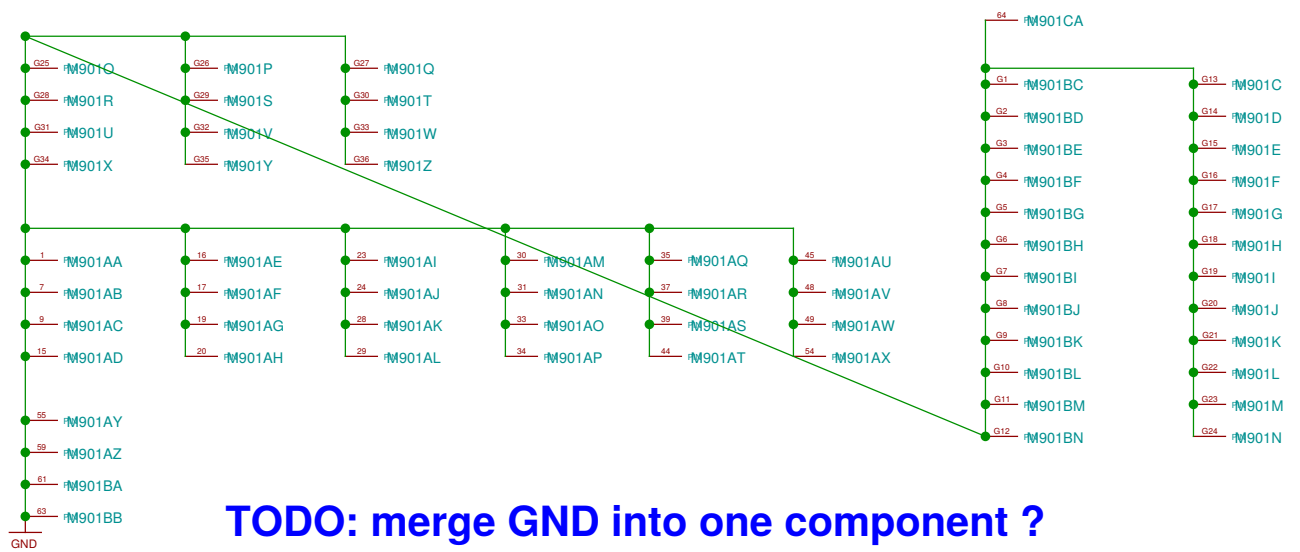
The RC filter should have C large enough enough to hold a charge in pulsed operation, yet be fast enough to detect short activity. With 10 kOhm and 1 nF, we get about 16 kHz.



TODO: complete comparator circuit
TODO: add silego i2c assignment
TODO: iox

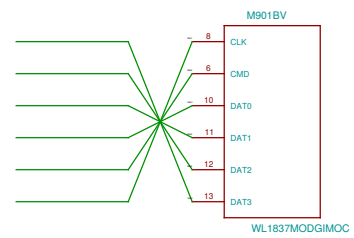
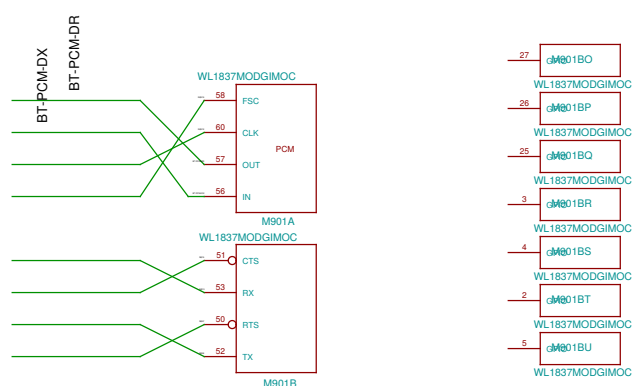


TODO: ANT2

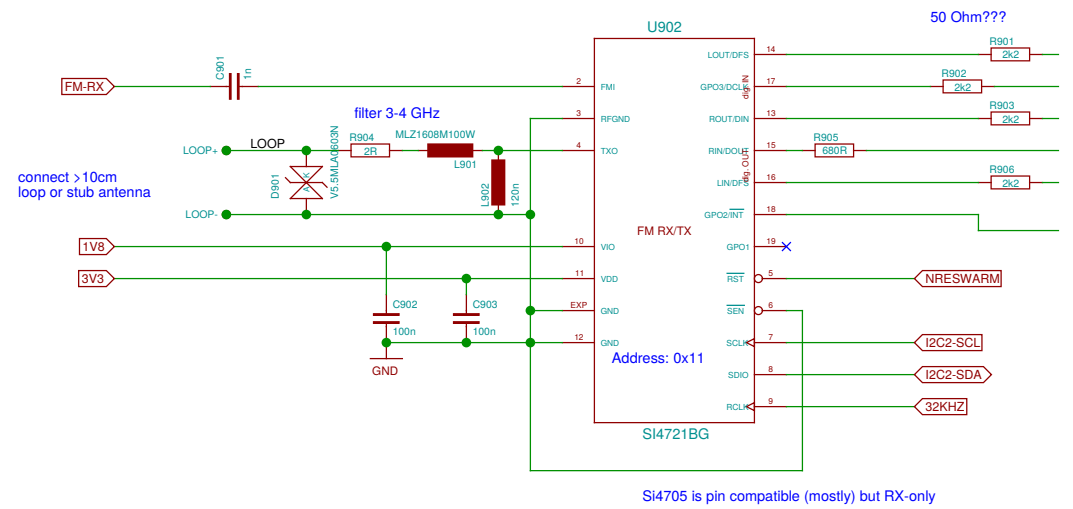


TODO: merge GND into one component ?

TODO: unfinished

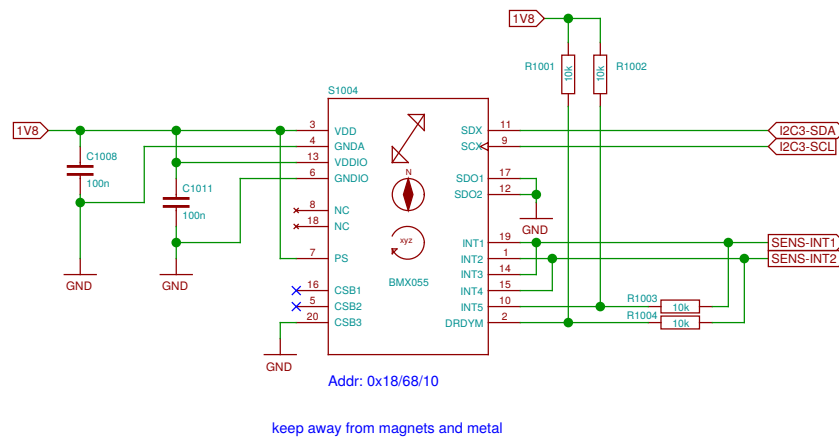
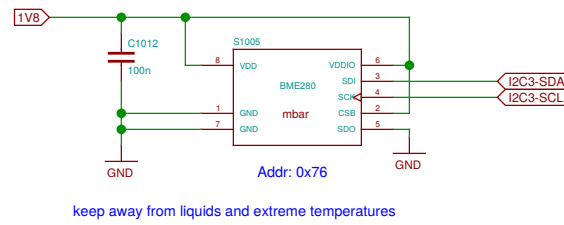
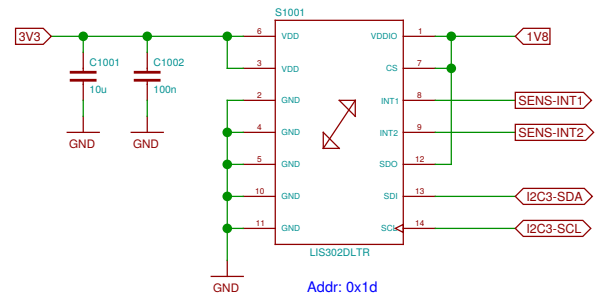


- _____ WLAN-IRQ
- _____ WLAN-EN
- _____ BT-EN
- _____ GPIO175
- _____ KEYIRQ



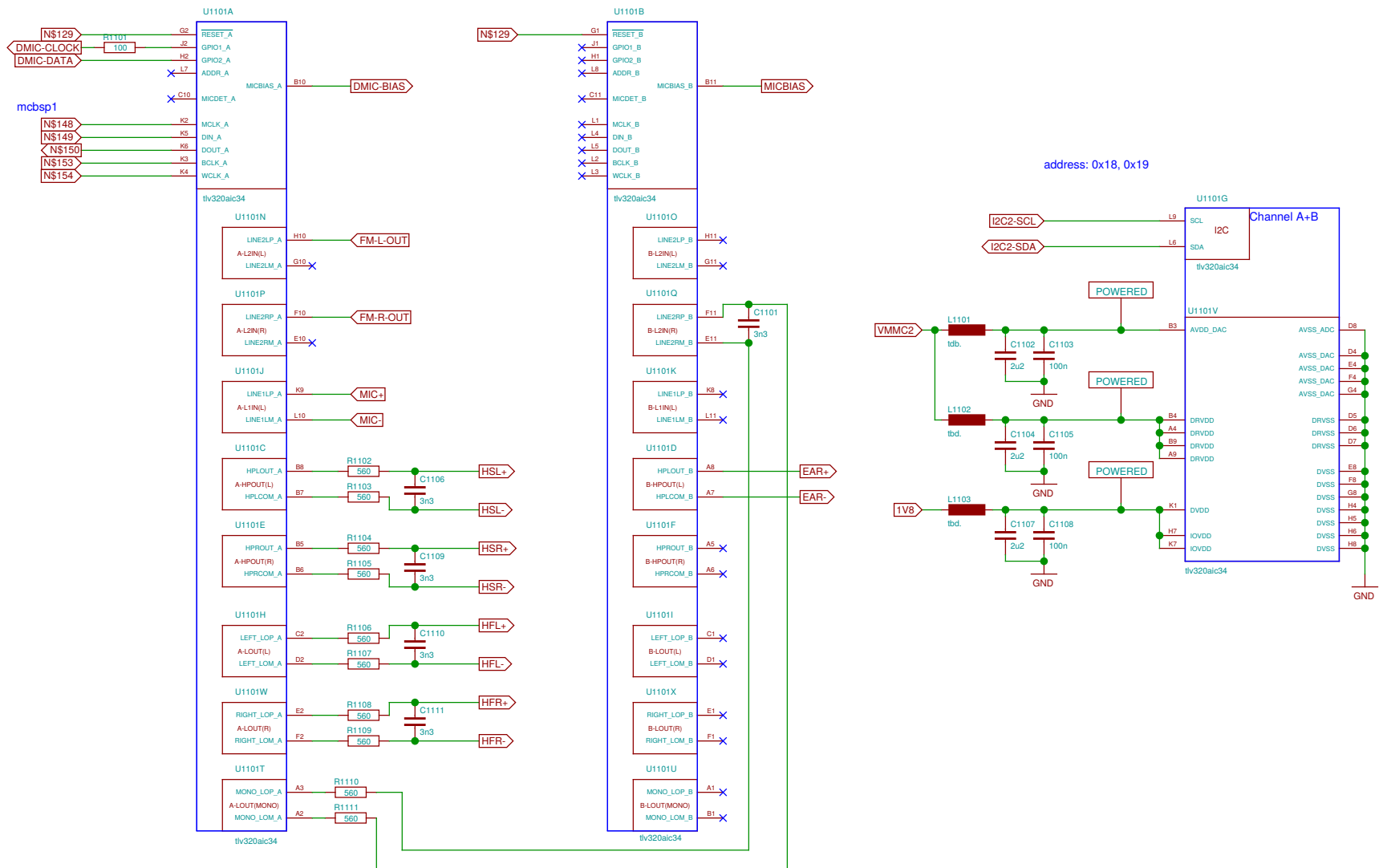
TODO: unfinished

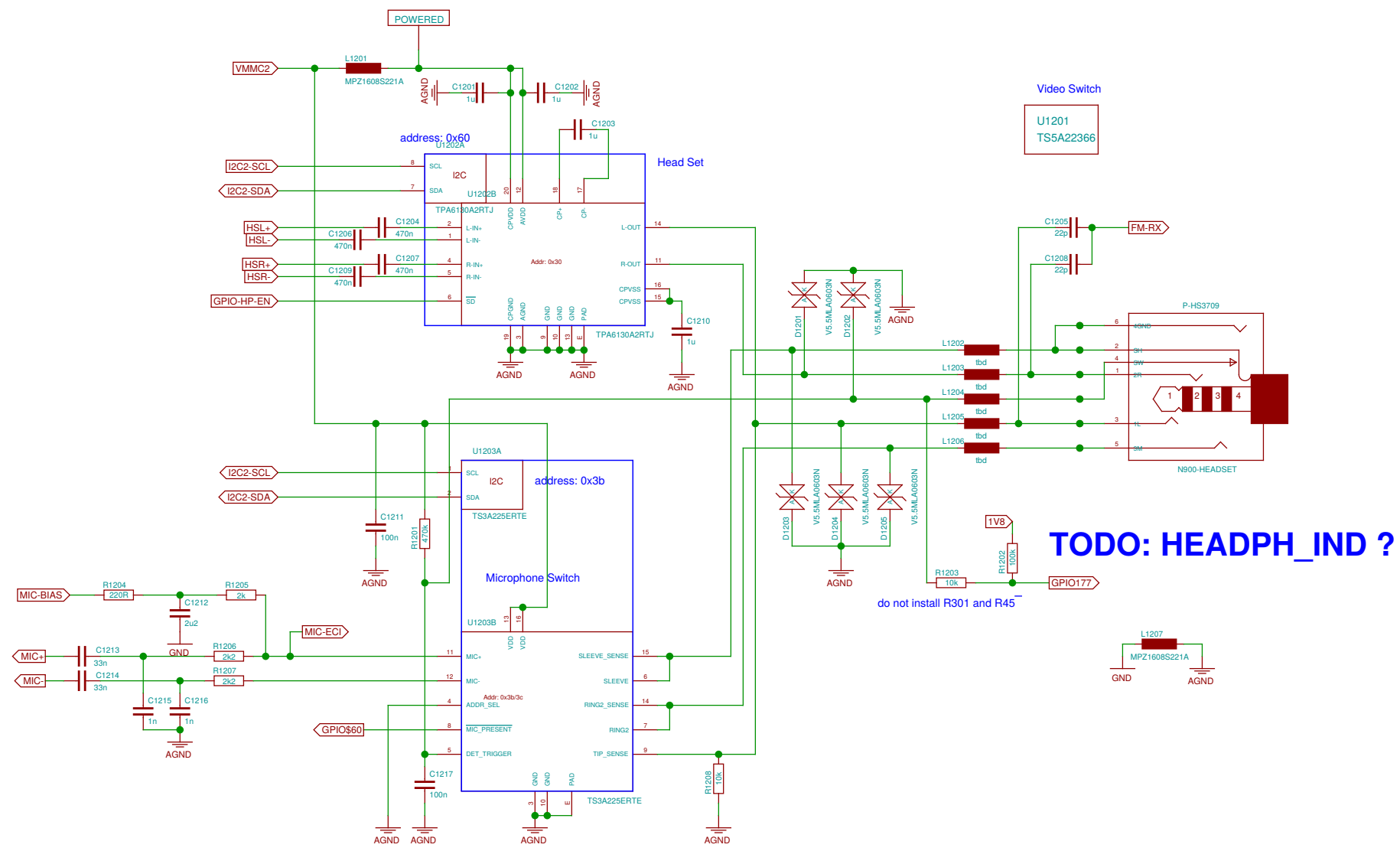
- FSX
- CLKX
- DX
- DR
- FSR
- CLKR



Sheet: /Sensors/ File: neo900_SS_10.sch		
Title: Sensors		
Size: A3	Date: 17 JUL 2016	Rev:
%K		Id: 10/37

problem: this is a 0.5mm BGA making lower board expensive
 but it appears to be not extremely critical (only 3 rows and inner ring is GND)
 problem: analog mic is on upper board
 alternative: place on upper board (to be evaluated)



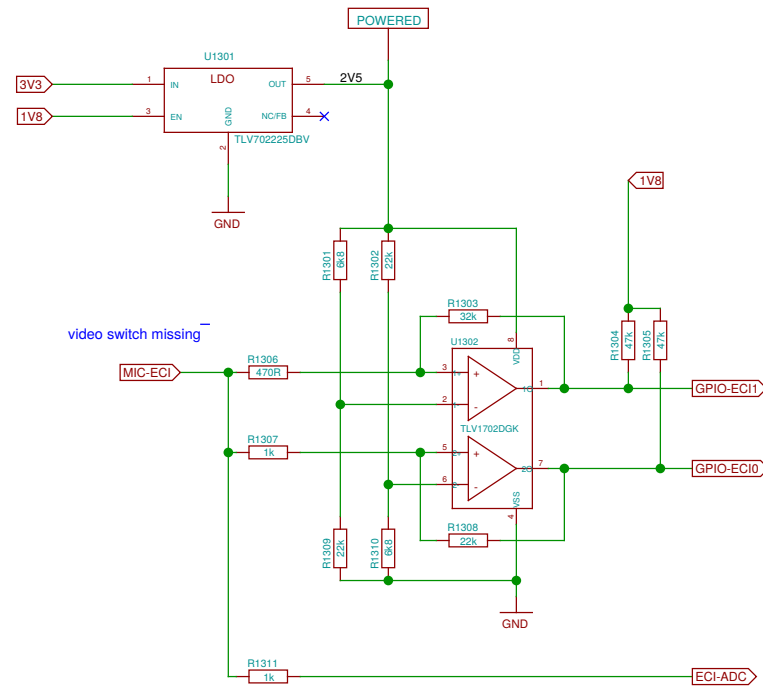


Video Switch
U1201
TS5A22366

TODO: HEADPH_IND ?

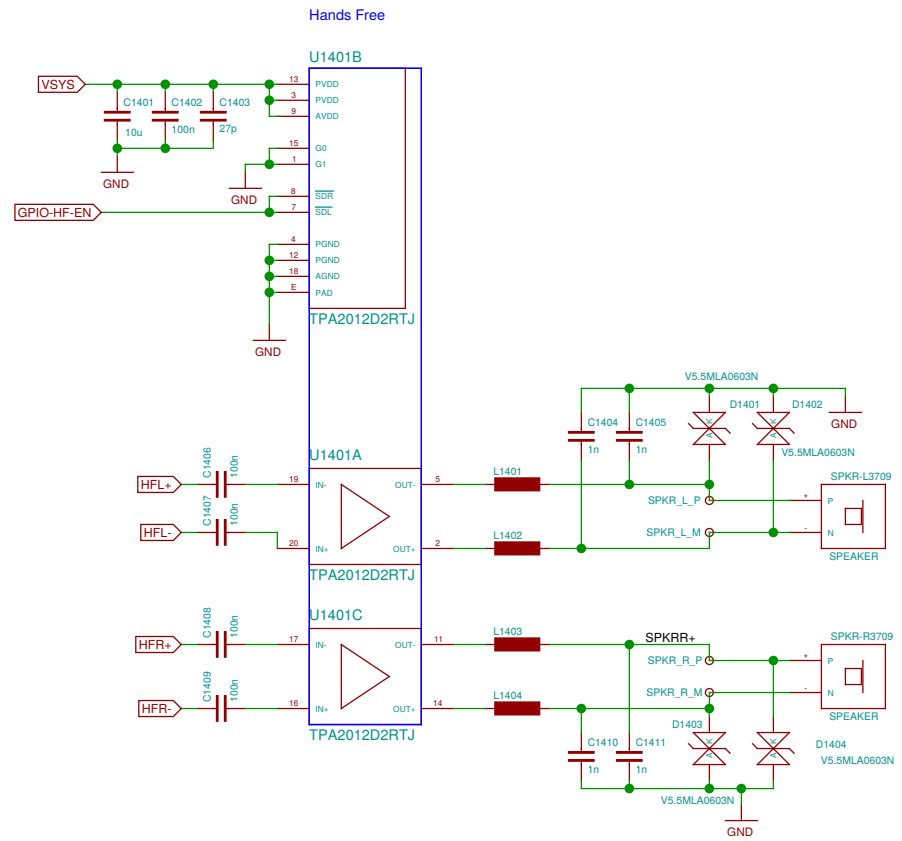
do not install R301 and R45

Sheet: /Audio Headset + Mic/ File: neo900_SS_12.sch		
Title: Audio Headset + Mic		
Size: A3	Date: 17 JUL 2016	Rev:
%K		Id: 12/37



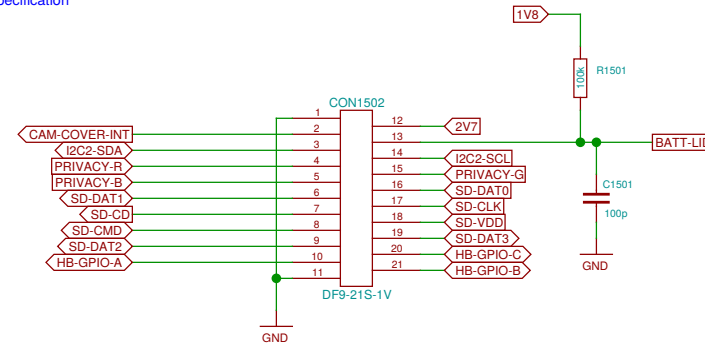
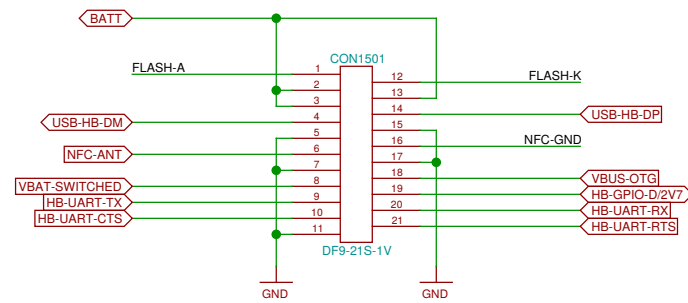
TODO: draw comparator right

Sheet: /ECI/		File: neo900_SS_13.sch	
Title: ECI			
Size: A3	Date: 17 JUL 2016	Rev:	
%K		Id: 13/37	



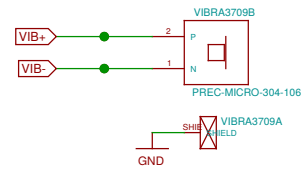
Sheet: /Audio Handsfree/		
File: neo900_SS_14.sch		
Title: Audio Handsfree		
Size: A3	Date: 17 JUL 2016	Rev:
%K		Id: 14/37

The LOWER-BOB interconnect is defined in the Hackerbus specification
<http://neo900.org/stuff/papers/hb.pdf>

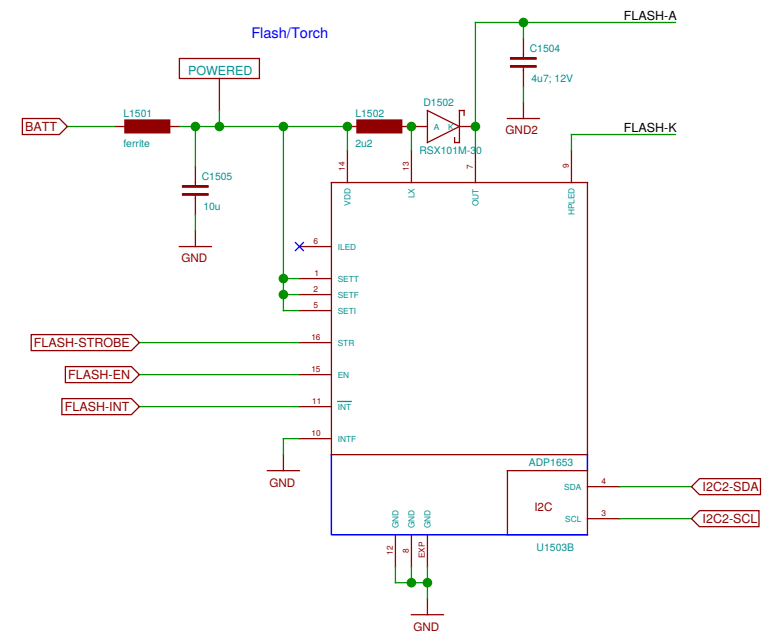
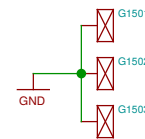


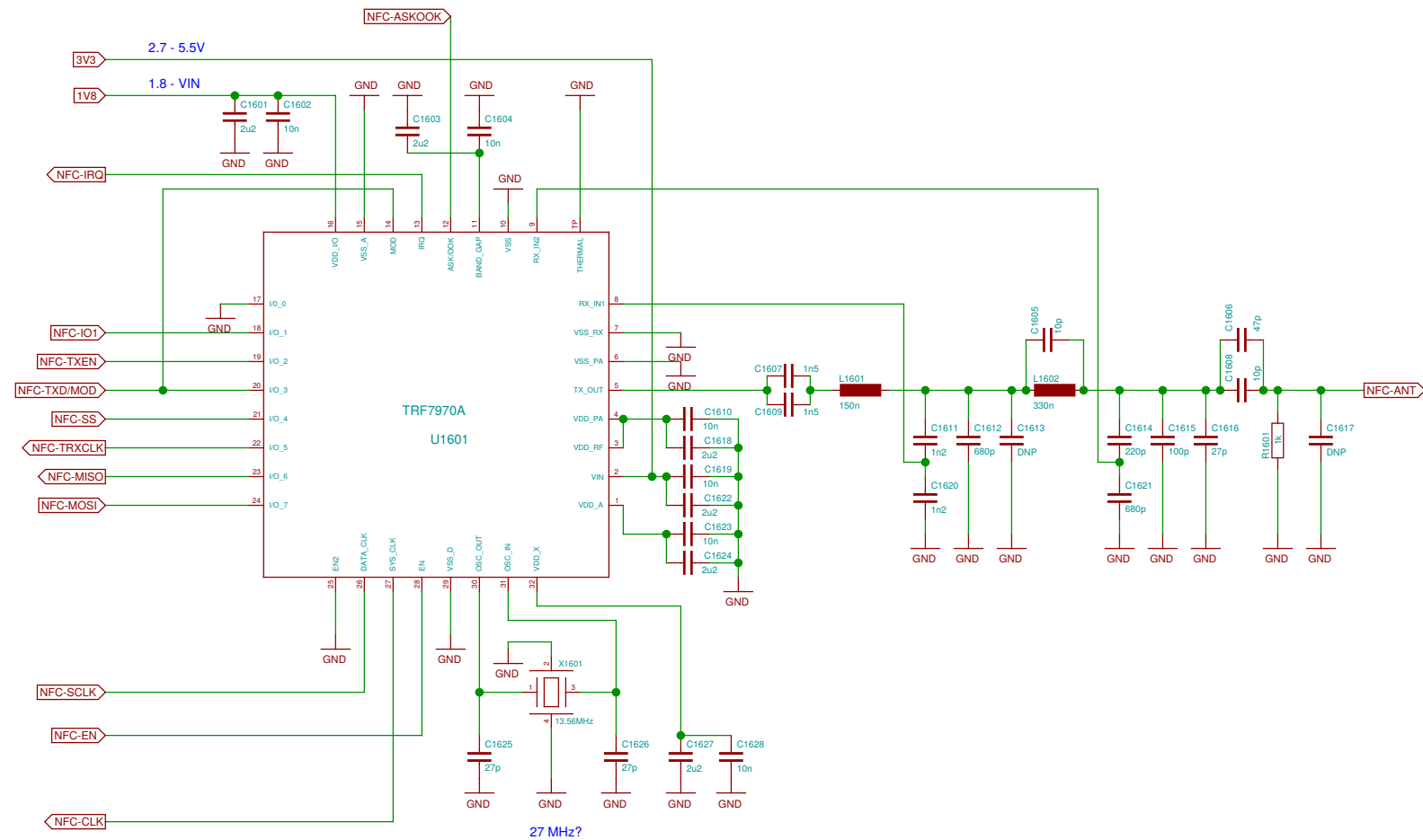
TODO: define NFC-GND

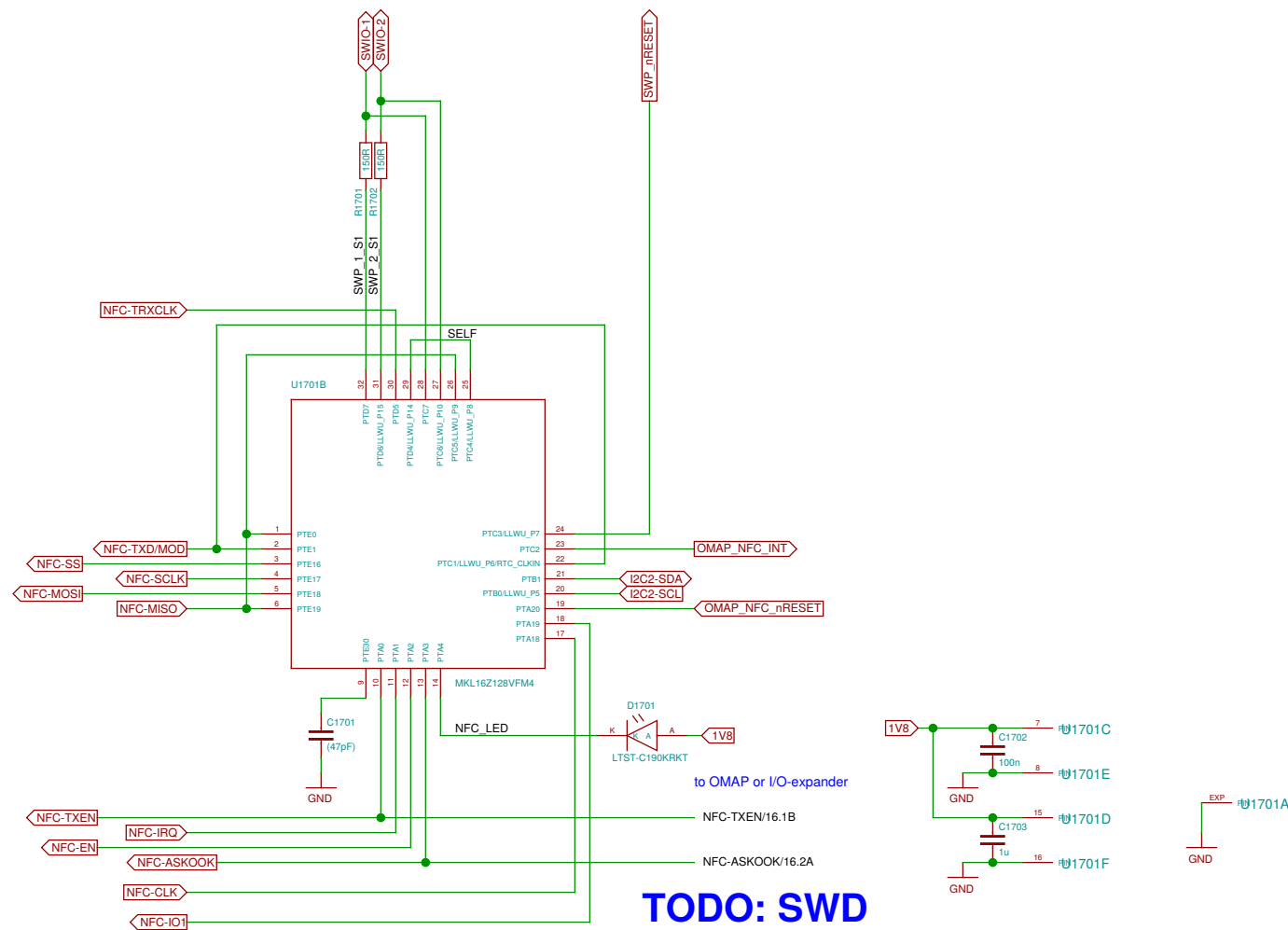
Vibramotor



Shield



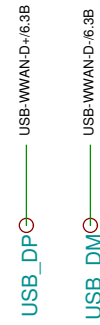




Sheet: /RFID/NFC Controller/		
File: neo900_SS_17.sch		
Title: RFID/NFC Controller		
Size: A3	Date: 17 JUL 2016	Rev:
%K		Id: 17/37

NOTE: this is mangling up Breakout and Lower board connectors
Signals may have to be fed through the breakout board connector increasing resistance

TODO: align with HB WP



TODO: HB "base circuit" (level shifters, etc.) goes here

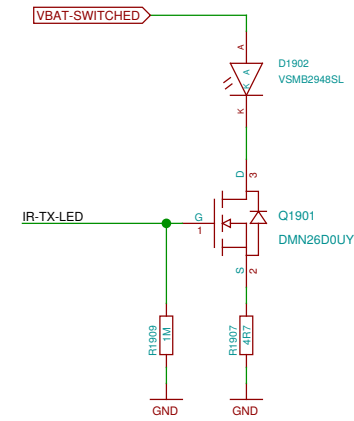
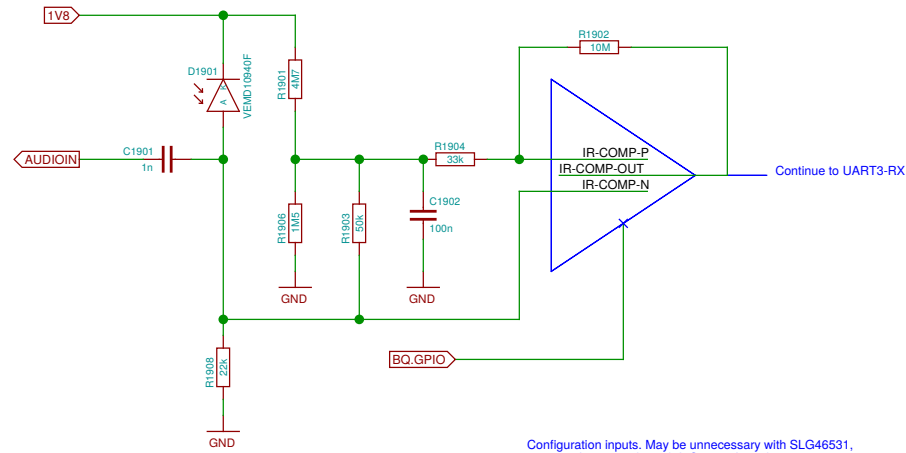
Missing 10 level shifter chip (or do we really have the space for 10x discrete T+R+D ca. 3x3mm each?)

Missing 6x 2R for alternate function select (do we have the space for ca. 2.5 x 5mm?)

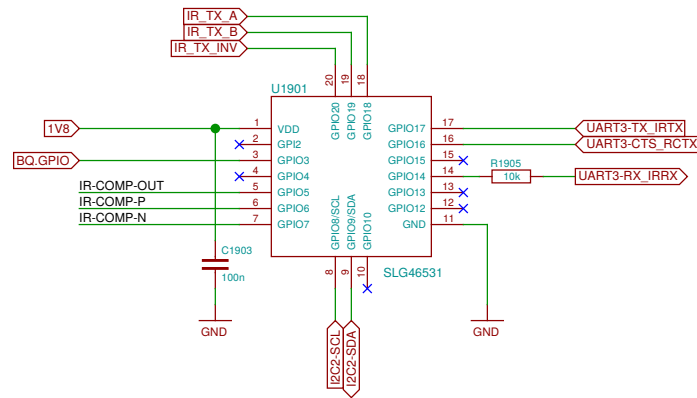
Sheet: /Hackerbus/ File: neo900_SS_18.sch	
Title: Hackerbus	
Size: A3	Date: 17 JUL 2016
%K	Rev: Id: 18/37

TODO: update D1901 footprint

NOTE: 1V8 may be quite noisy



Configuration inputs. May be unnecessary with SLG46531, once configuration through I2C is confirmed.

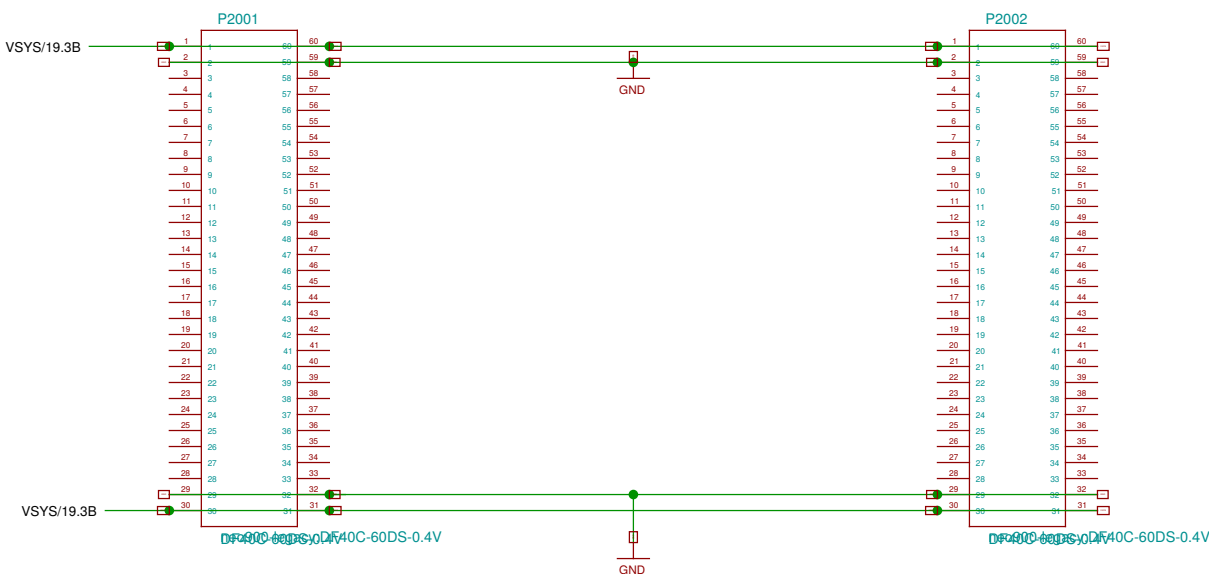


TODO: update when details settle

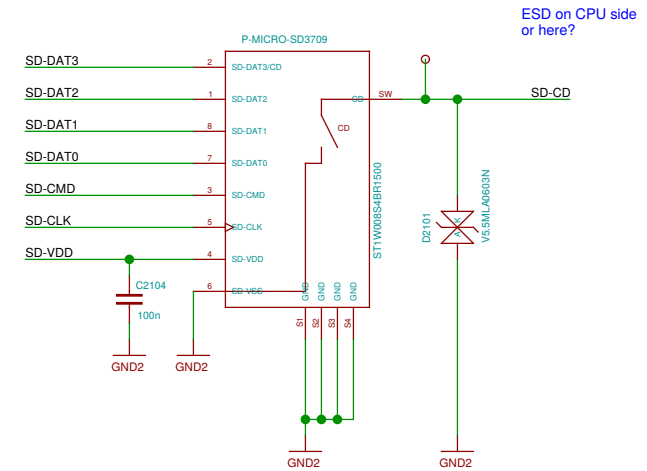
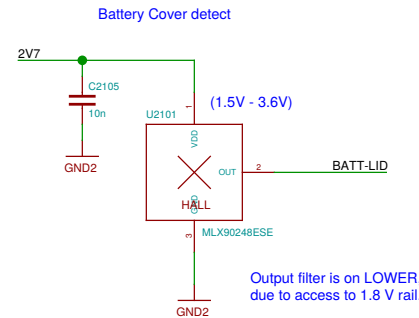
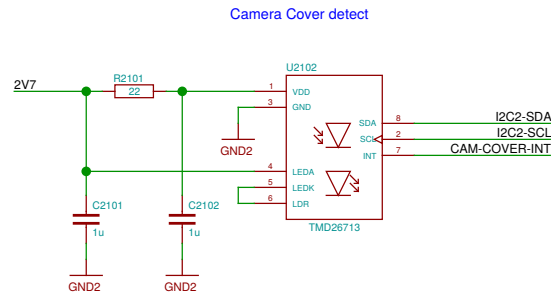
ca. 130 signals (to be counted exactly after definition of upper/lower split)

- MMCS-DATA1/9.1A
- MMCS-DATA2/9.1A
- MMCS-DATA3/9.1A
- GPIO-WLAN-IRQ/9.1A
- GPIO-BT-EN/9.1C
- UART1-RX/9.1C
- UART1-RTS/9.1C
- UART1-CTS/9.1D
- UART1-TX/9.1D
- MCBSP3-FCK/9.1D
- MCBSP3-CLK/9.1D
- MCBSP3-DR/9.1D
- MCBSP3-DX/9.1D
- SYSCLK/9.3C
- 32KHZ/9.4A
- GPIO-FM-EN/9.3A
- GPIO-FMIRQ/9.3A
- MCBSP2-FCK/9.3A
- MCBSP2-CLK/9.3A
- MCBSP2-DR/9.3A
- MCBSP2-DX/9.3A
- GPIN115/10.3B
- GPIO56/10.3A
- GPIO51/10.3B
- GPIO55/10.4A
- GPIO56/10.4A
- ACCEL-INT/10.4C
- NS129/11.2A
- NS148/11.1A
- NS149/11.1A
- NS150/11.1A
- NS153/11.1A
- NS154/11.1A
- GPIO-ECI1/13.3B
- GPIO-ECI0/13.3C
- ECI-ADC/13.3C
- VMMC2/12.1A
- GPIO-HP-EN/12.1B
- GPIO50/12.2D
- GPIO177/12.4C
- GPIO-HF-EN/14.1B
- GPIO-FLASH-STR/15.1A
- GPIO-FLASH-EN/15.1A
- GPIO-FLASH-INT/15.1A
- GPIO-BATT-LID/15.1B
- SD-CMD/15.2A
- SD-CLK/15.2A
- SD-CD/15.2B
- SD-VDD/15.2A
- SD-DAT0/15.2B
- SD-DAT1/15.2B
- SD-DAT2/15.2A
- SD-DAT3/15.2A
- VIB+/15.1D
- VIB-/15.1D
- 3V3/19.1D
- 2V5/13.3B
- 1V8/19.1D
- VBUS/18.1C
- OTG-D-/3.1B
- OTG-D+/3.1B
- OTG-ID/2.2B
- VBUS-MODEM/6.3B
- USB-WWAN-D+/18.3A
- USB-WWAN-D-/18.3A
- 2V7/8.4C
- GPIO-CAM-COVER/15.1B
- NS38
- LOCK-GPIO/1.2A
- POWERON/1.3A
- GPIO-VOL+/1.2B
- GPIO-VOL-/1.2B
- CAM1-GPIO/1.3B
- CAM2-GPIO/1.3C
- I2C3-SDA/10.4C
- I2C3-SCL/10.4C
- CHG_IND/3.1B
- NS131/3.1C
- NS141/3.1C
- NS143/3.1C
- BATTEMP/5.4A
- GPIO-EN-MODEM/4.1A
- I2C2-SDA/15.1A
- I2C2-SCL/15.1A
- INA231-INT/4.4C
- HDO/5.2A
- GPIO570/8.3B
- GPIO5110/8.1D
- NS19/8.2D
- NS229/8.3C
- ADC5114/8.1C
- ADC1/8.4C
- ADC2/8.4C
- GPIO-COMPARATOR/8.4D
- MCBSP4-DR/6.2A
- MCBSP4-DX/6.2A
- MCBSP4-CLKX/6.2A
- MCBSP4-FSX/6.2A
- UART7-RTS/6.2C
- UART7-CTS/6.2C
- UART7-RX/6.2C
- UART7-TX/6.2C
- RING/6.2C
- GPIO-MODEM_IGT/6.3A
- GPIO-MODEM_EMERG/6.3A
- EMERG_OFF/6.3B
- PWR_IND/6.3B
- LC_IND/6.3B
- STATUS/6.3B
- 3G-WOE/6.3B
- GPIO52/8.4A
- GPIO-WLAN-EN/9.1A
- MMCS-CLK/9.1A
- MMCS-CMD/9.1A
- MMCS-DATA0/9.1A

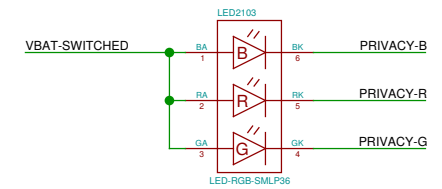
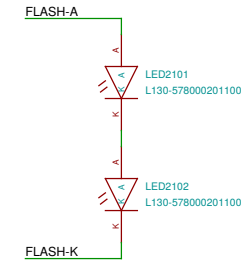
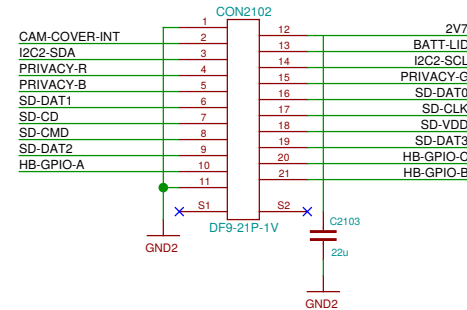
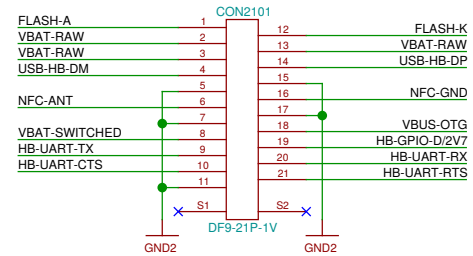
Pin assignment must be optimized for final component placement
we might have to switch to 80 or 100 pin connectors



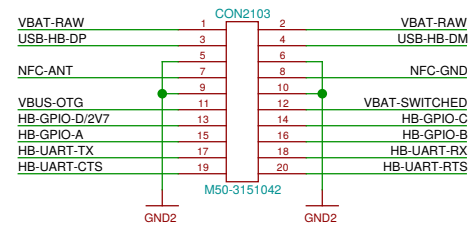
TODO: add ESD protection (here)



The LOWER_BOB interconnect is defined in the Hackerbus specification
<http://neo900.org/stuff/papers/hb.pdf>

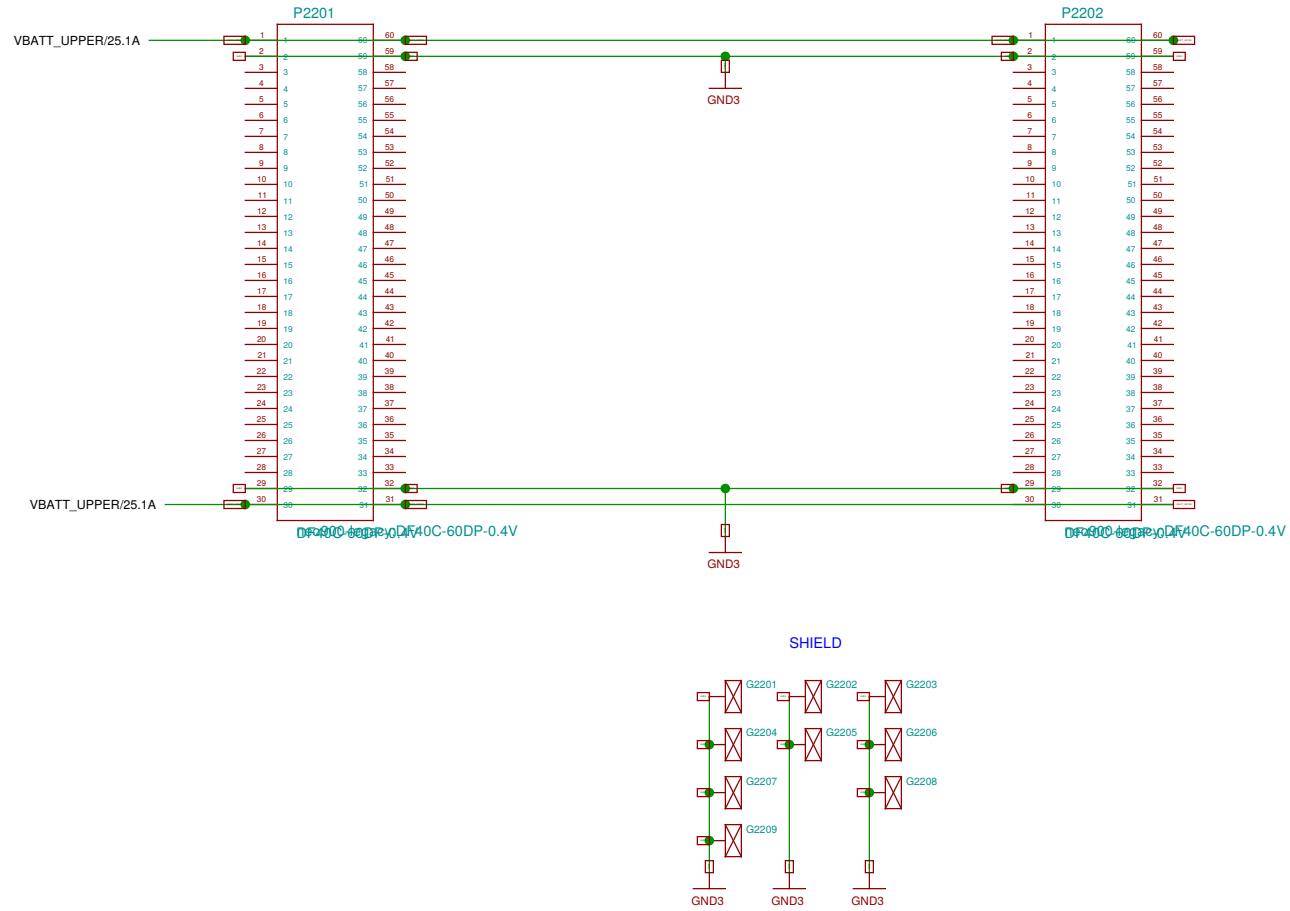


Hackerbus



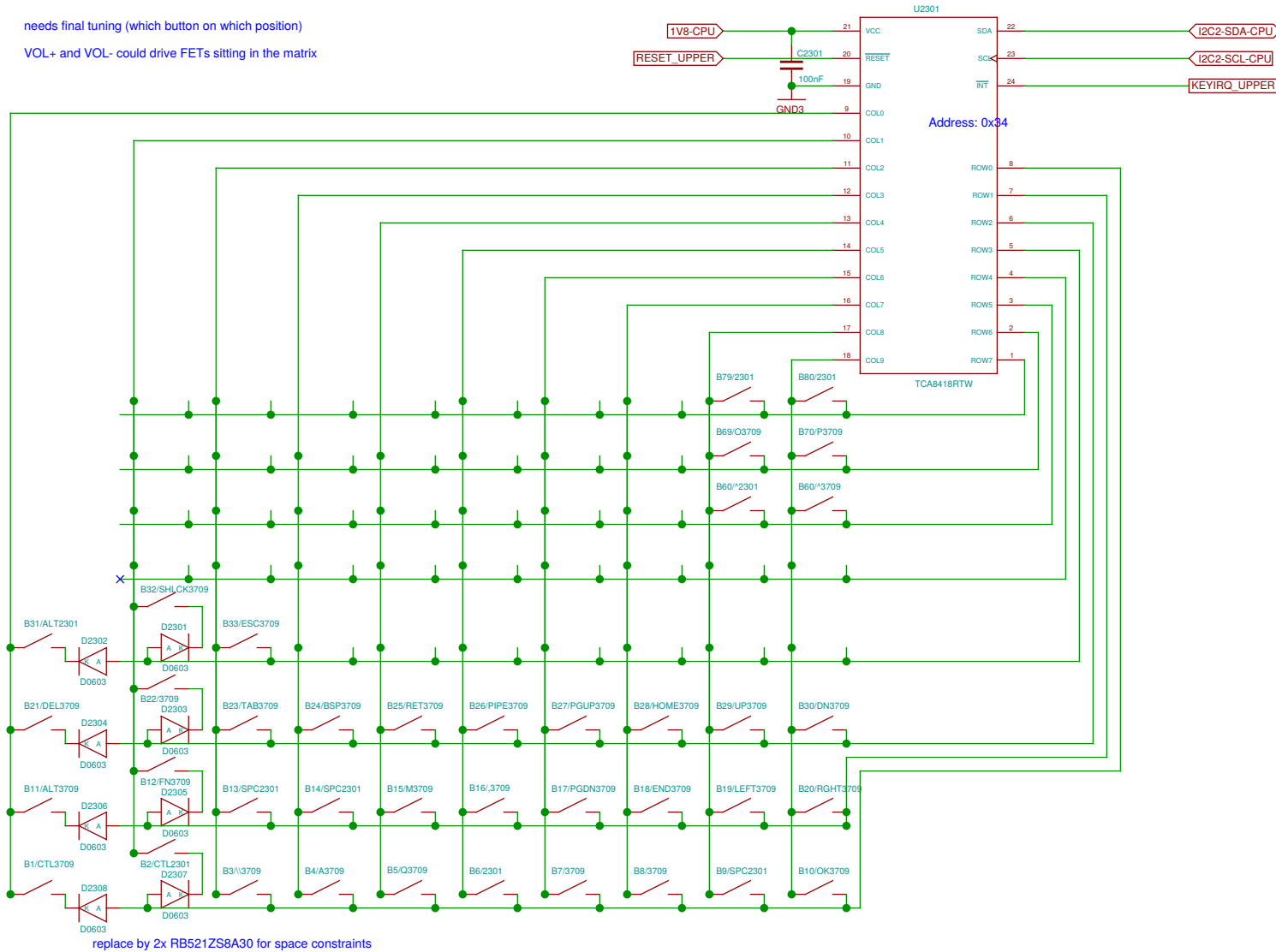
TODO: track B2B to UPPER

to be adjusted to lower board connector



TODO: *_UPPER names ?

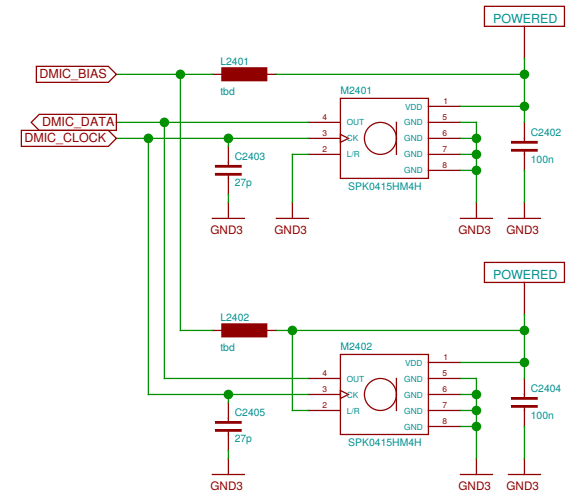
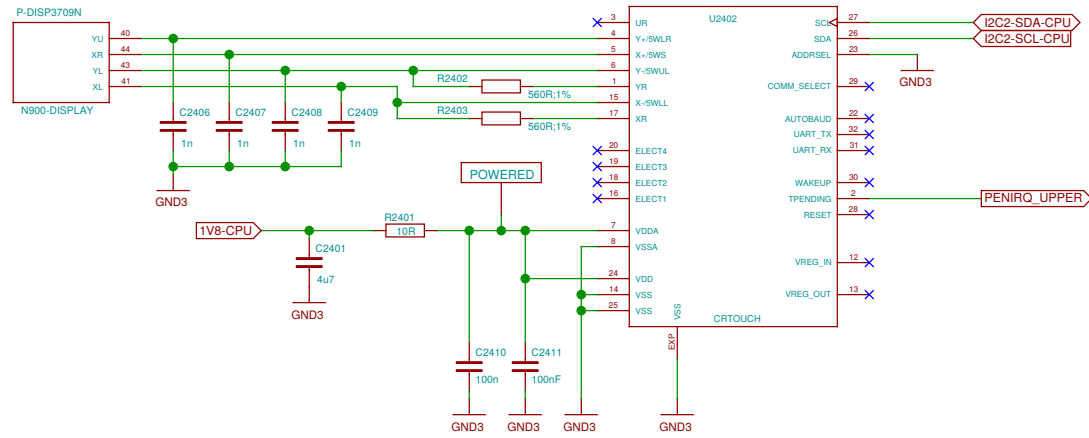
needs final tuning (which button on which position)
 VOL+ and VOL- could drive FETs sitting in the matrix



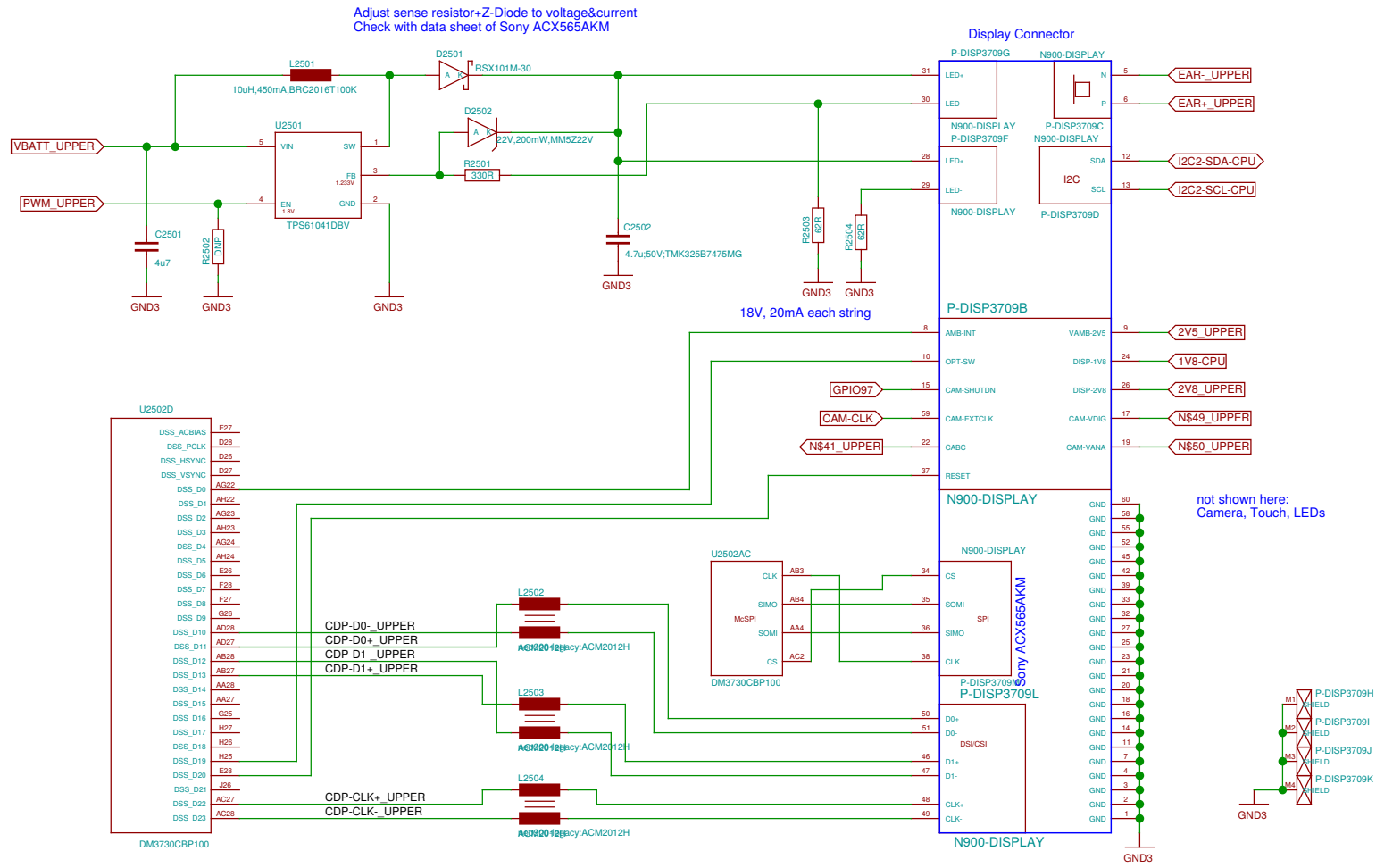
replace by 2x RB521ZS8A30 for space constraints

- TODO: remove 3709 in comp ref
- TODO: remove keycap from comp ref
- TODO: sort out 6 "ext" buttons
- TODO: rearrange matrix to avoid diodes ?

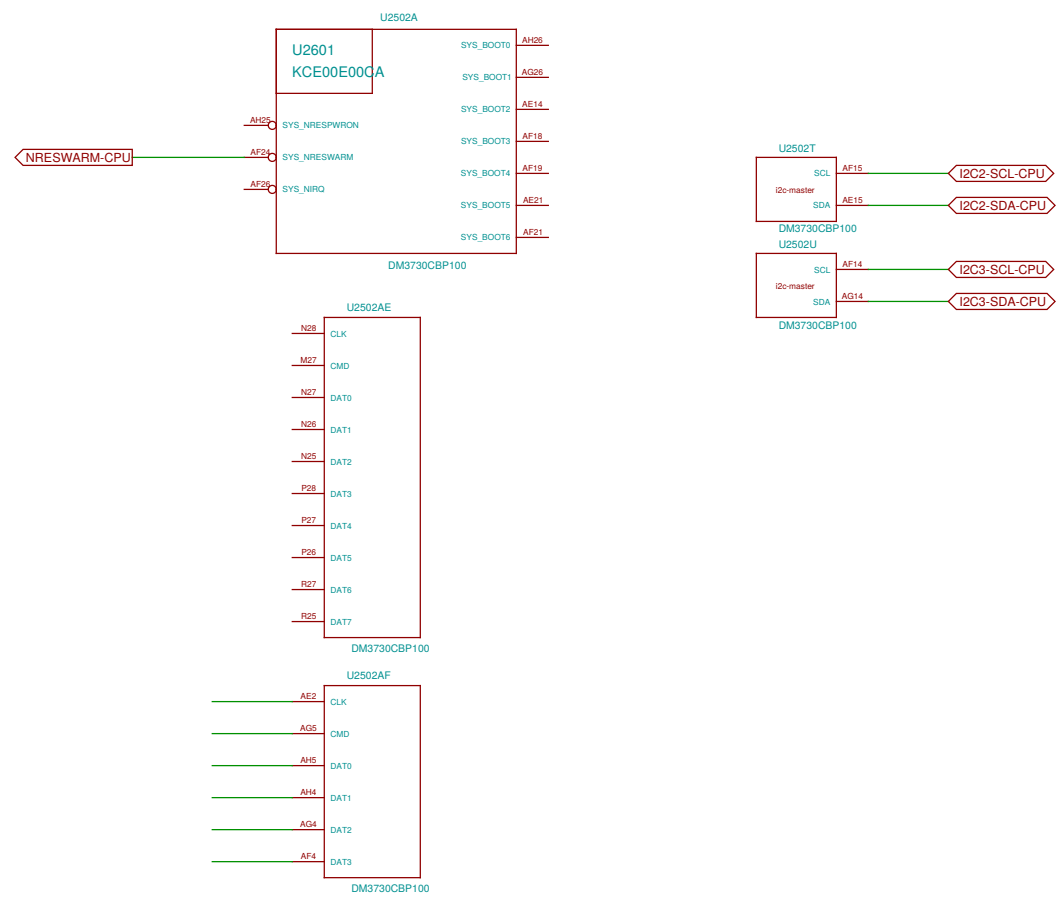
Resistive Touch (display connector)



TODO: connector pin assignment needs intensive review

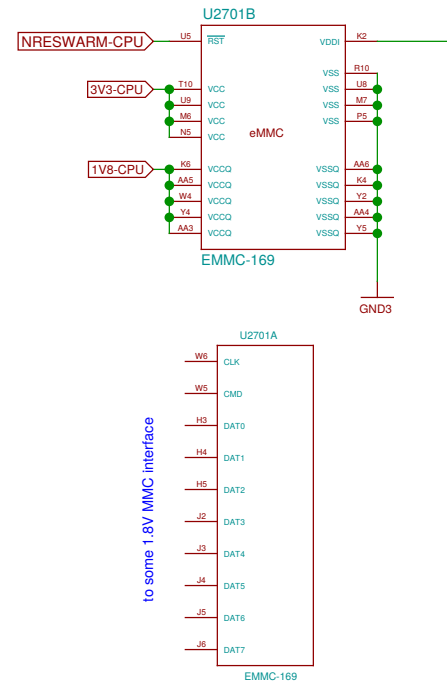


INCOMPLETE in V2



Sheet: /CPU + PoP RAM/NAND/ File: neo900_SS_26.sch		
Title: CPU + PoP RAM/NAND		
Size: A3	Date: 17 JUL 2016	Rev:
%K		Id: 26/37

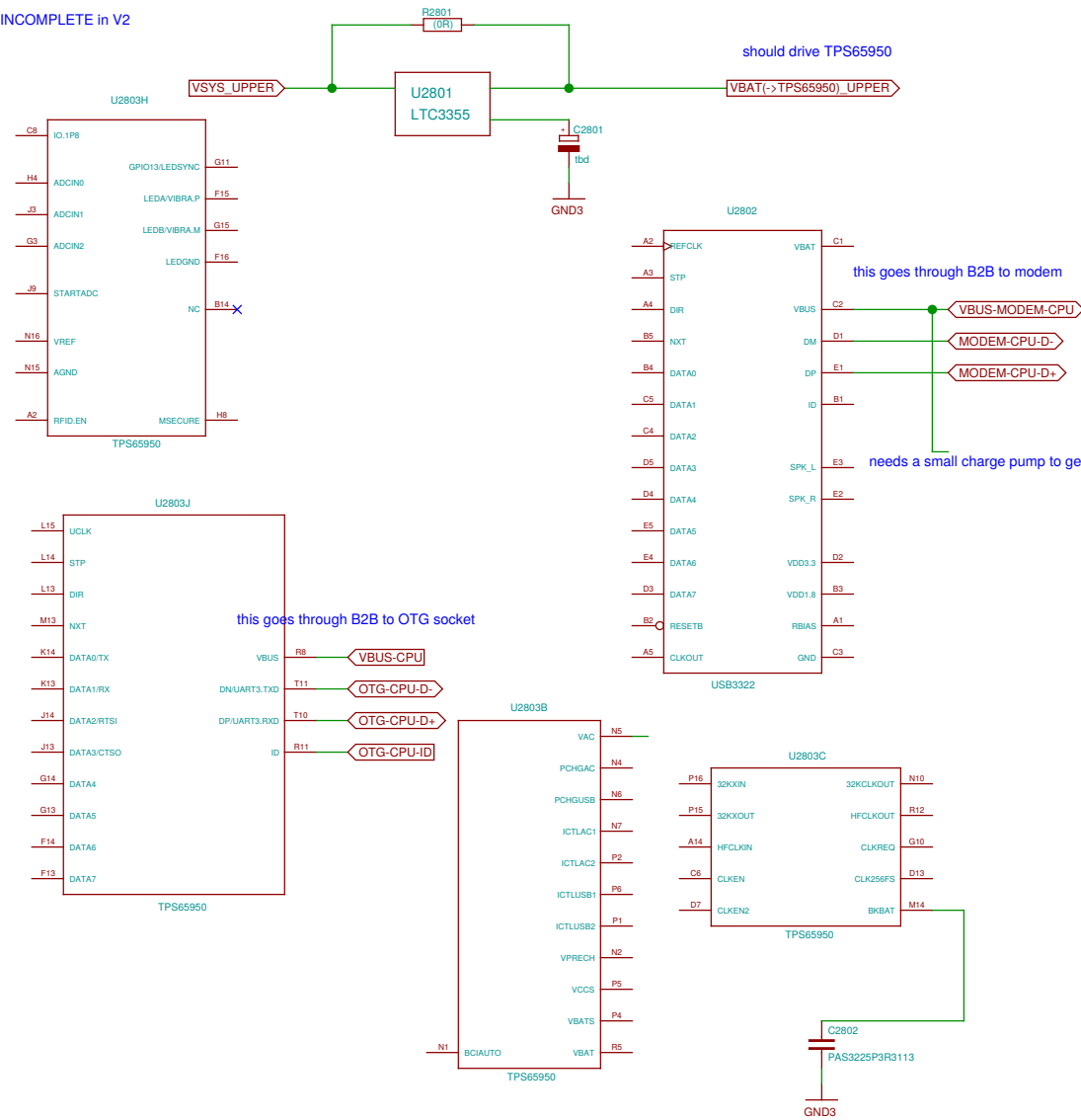
INCOMPLETE in V2



Sheet: /eMMC/ File: neo900_SS_27.sch		
Title: eMMC		
Size: A3	Date: 17 JUL 2016	Rev:
%K		Id: 27/37

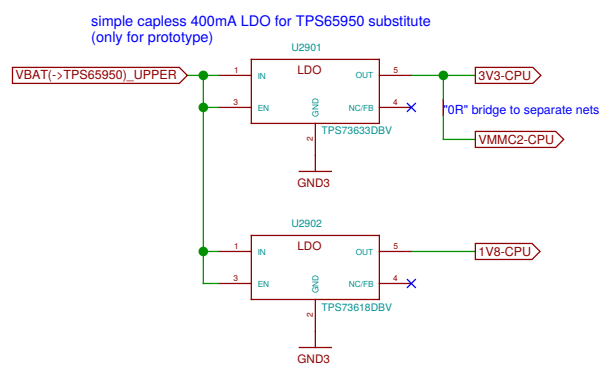
TODO: check role

INCOMPLETE in V2



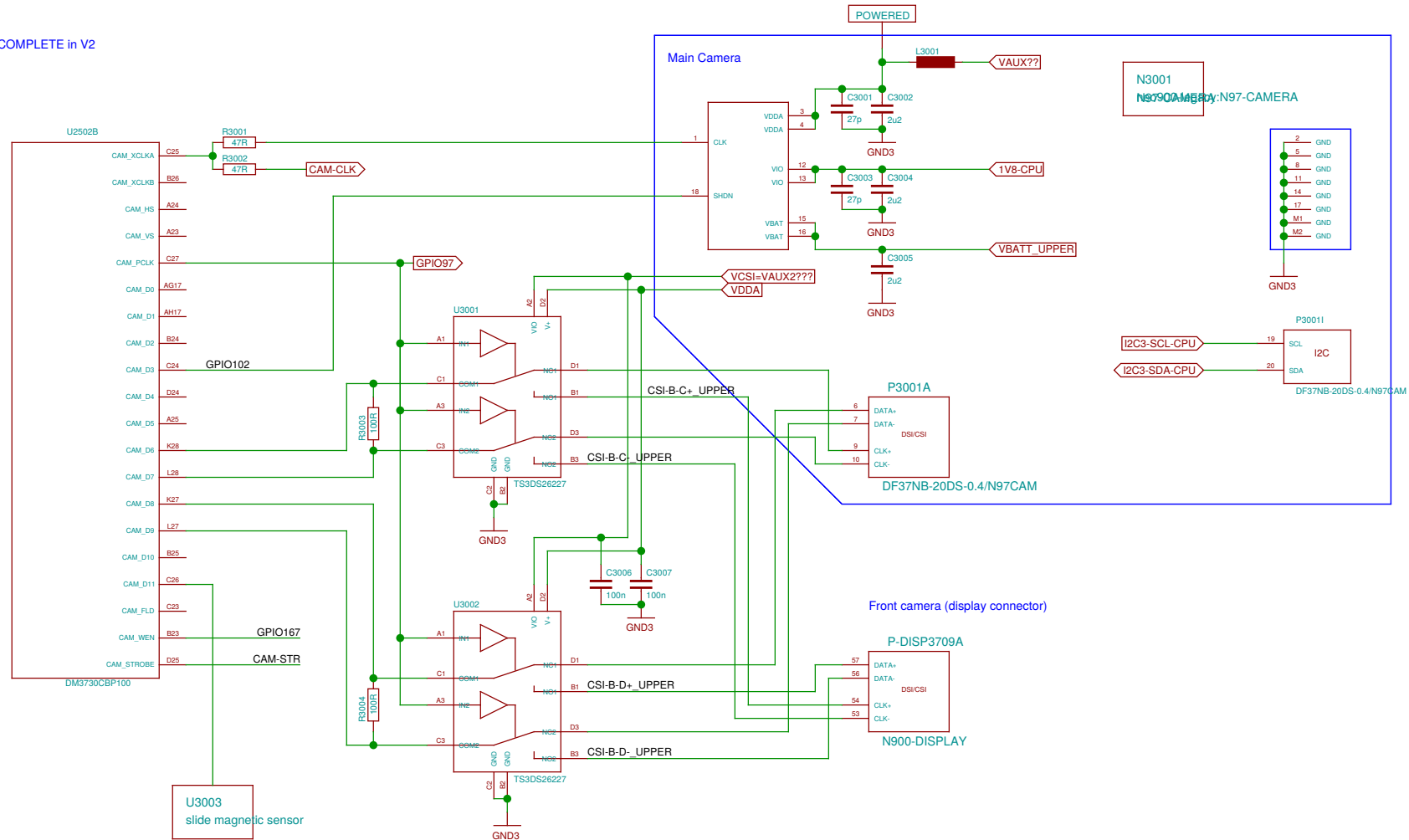
TODO: VBUS-MODEM ?

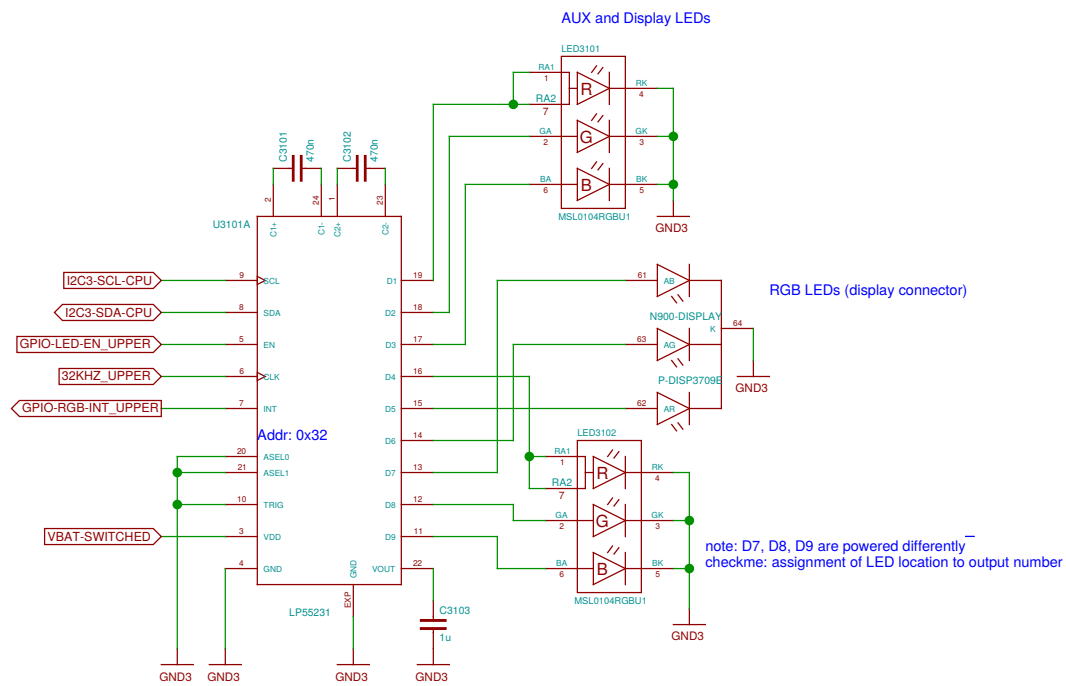
Sheet: /PMU+Codec/		
File: neo900_SS_28.sch		
Title: PMU+Codec		
Size: A3	Date: 17 JUL 2016	Rev:
%K		Id: 28/37



Sheet: /BB-XM Dummy (TWL4030)/		File: neo900_SS_29.sch	
Title: BB-XM Dummy (TWL4030)			
Size: A3	Date: 17 JUL 2016	Rev:	
%K		Id: 29/37	

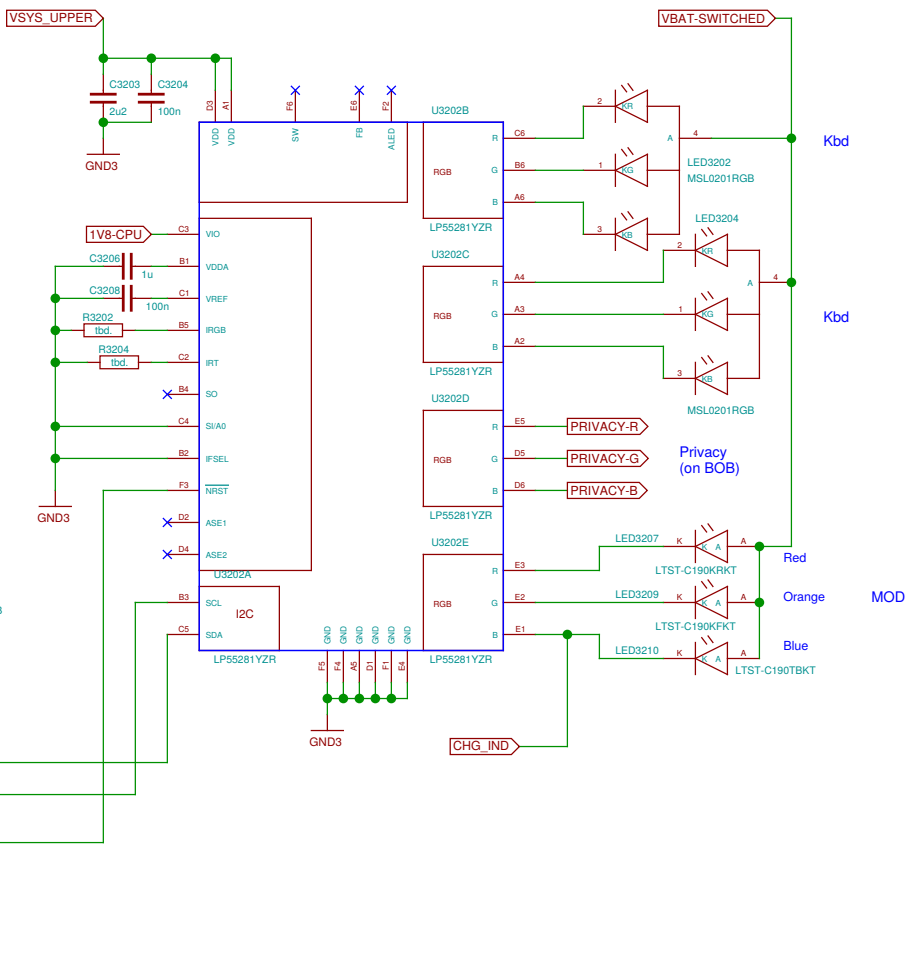
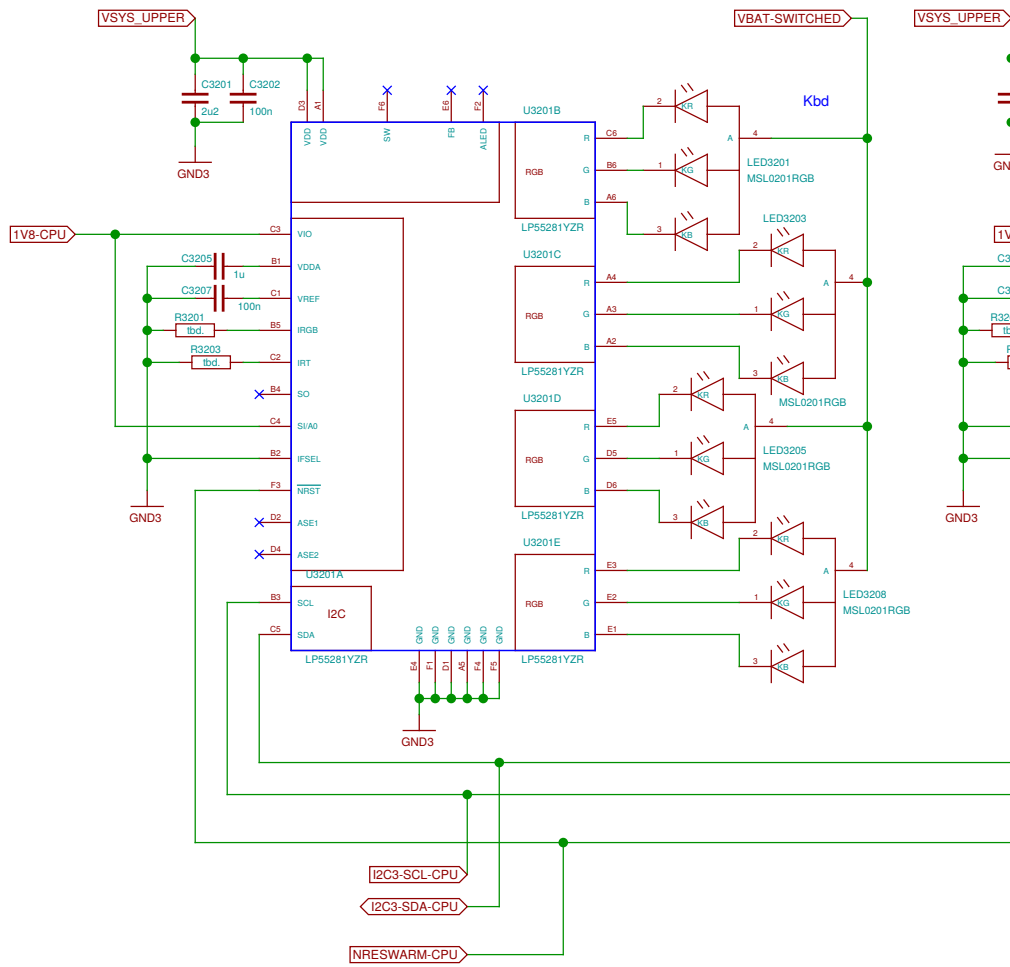
INCOMPLETE in v2





TODO: LEDs/Fancy LEDs sheets have title swapped

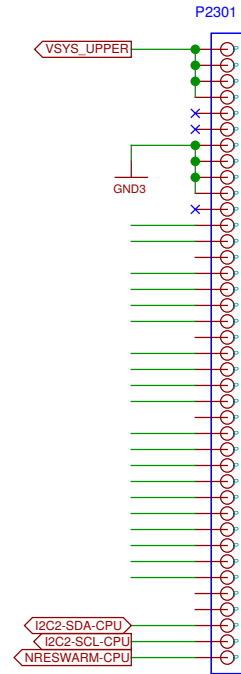
Sheet: /LEDs/ File: neo900_SS_31.sch		
Title: LEDs		
Size: A3	Date: 17 JUL 2016	Rev:
%K		Id: 31/37



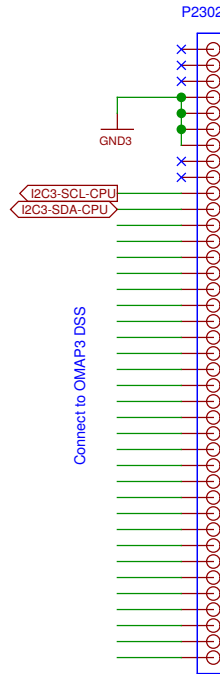
These connectors allow to "emulate" the DM3730 by connecting a BB-XM

INCOMPLETE
prototype only

Connect to OMAP3 McSPI1, I2C2, MMC2 / some GPIOs



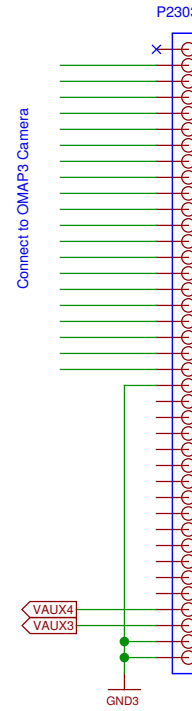
connect to respective CPU-pads



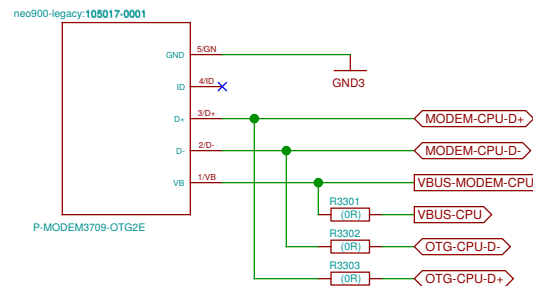
Connect to OMAP3 DSS

DSS / GPIOs, I2C3

Connect to OMAP3 Camera

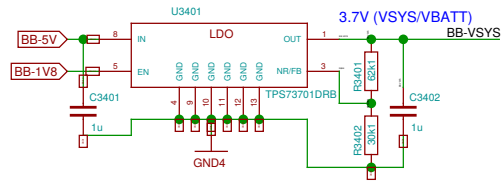


connect to BB
by some Micro-USB cable

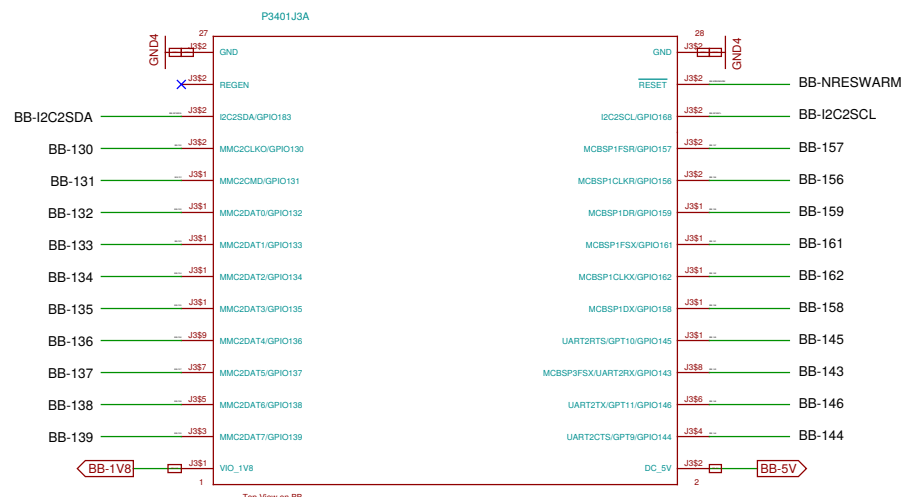
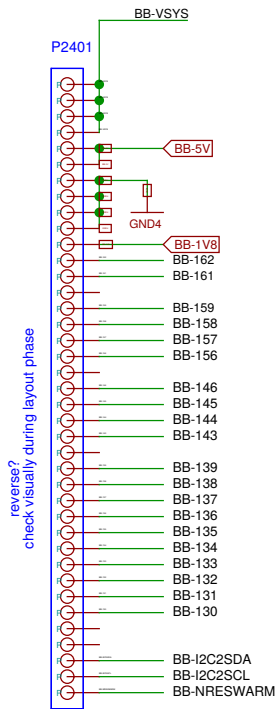


TODO: VBUS-MODEM ?

Sheet: /Connector to BB-XM/ File: neo900_SS_33.sch	
Title: Connector to BB-XM	
Size: A3	Date: 17 JUL 2016
%K	Rev: Id: 33/37

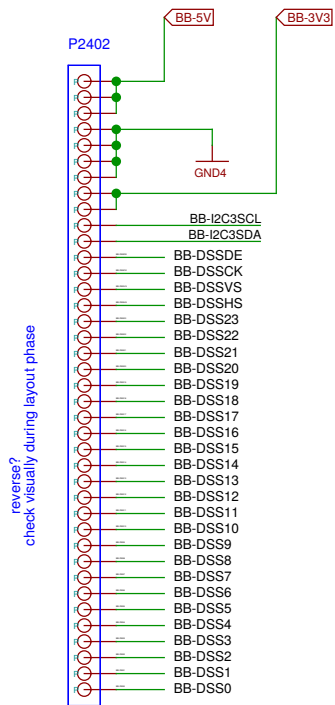


Ersetzen durch 2A buck converter

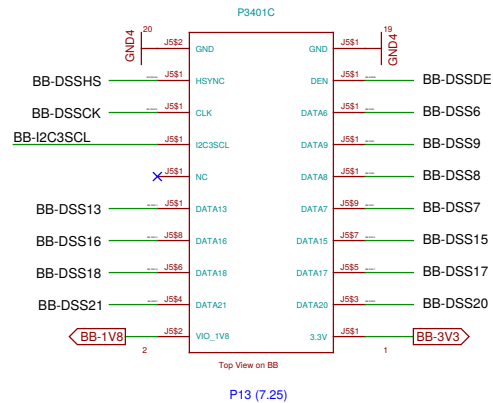
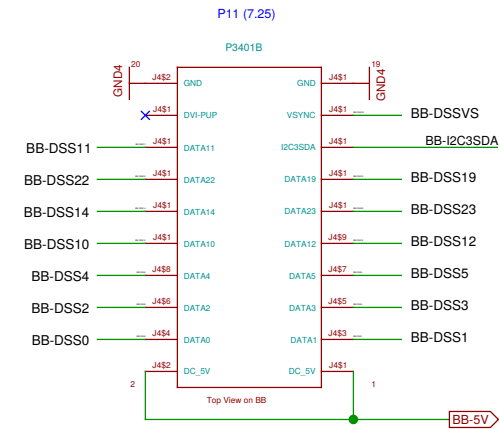


BB-xM Main Expansion Header (7.24)

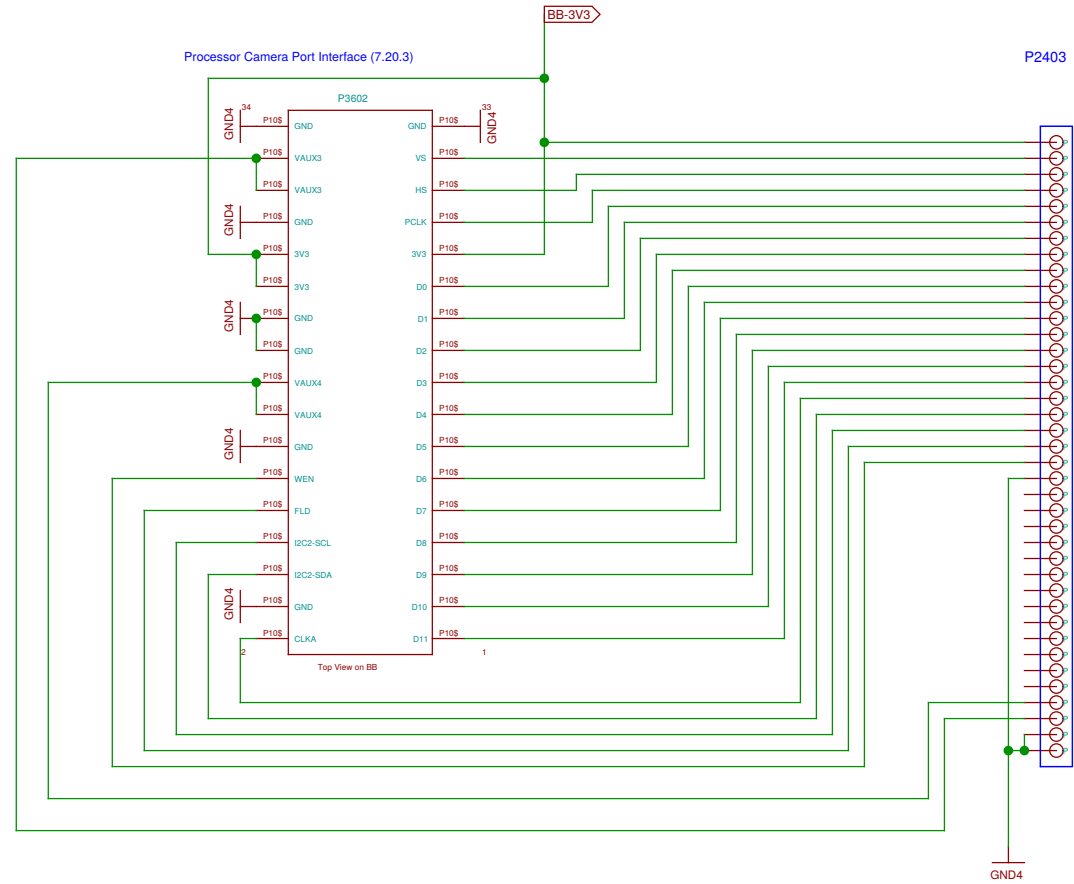
TODO: needs decision on where to take this



reverse?
check visually during layout phase



TODO: needs decision on where to take this



reverse?
check visually during layout phase

Sheet: /BB-XM Adapter (CAM)/		
File: neo900_SS_36.sch		
Title: BB-XM Adapter (CAM)		
Size: A3	Date: 17 JUL 2016	Rev:
%K		Id: 36/37

Molex Jumper cables to connect BB-XM-Adapter to Uppwer board

N3701 15015-0439	N3702 15015-0439	N3703 15015-0439
CPU	DISP	CAM

N3704 N900 case assembly

N3705 N97-CAMERA-HOLE

N3706 headset jack

N3707 STENCIL-TOP

N3708 STENCIL-BOTTOM

Sheet: /No-Solder Components/ File: neo900_SS_37.sch		
Title: No-Solder Components		
Size: A3	Date: 17 JUL 2016	Rev:
%K		Id: 37/37