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CPU + PoP RAM/NAND

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Connector to BB-XM

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BB-XM Adapter (CPU)

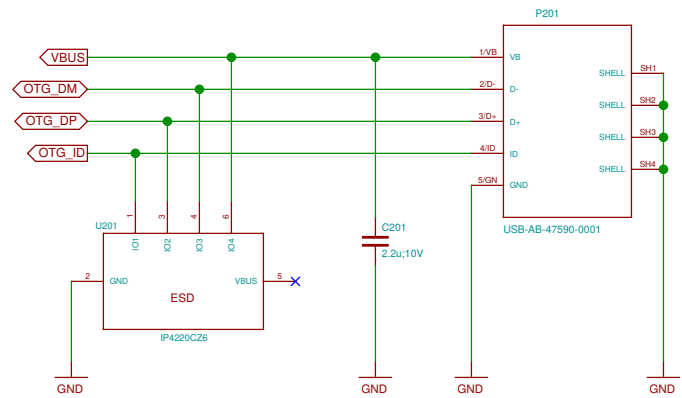
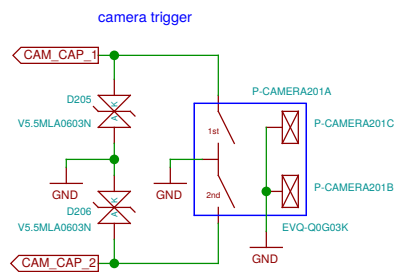
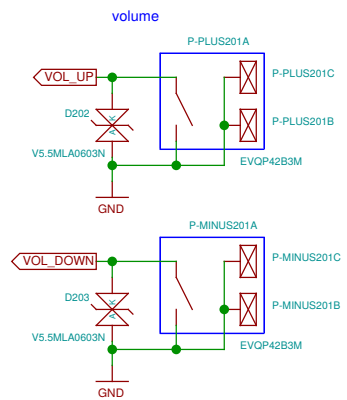
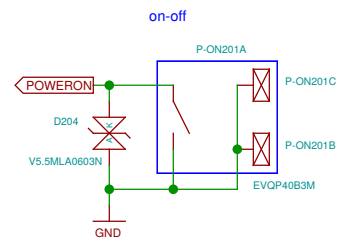
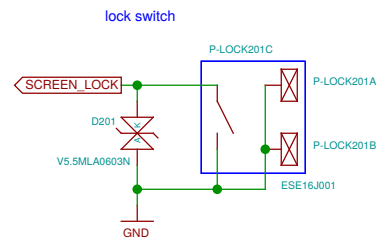
[Sheet: BB-XM Adapter \(DISP\)](#)
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BB-XM Adapter (DISP)

[Sheet: BB-XM Adapter \(CAM\)](#)
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BB-XM Adapter (CAM)

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No-Solder Components

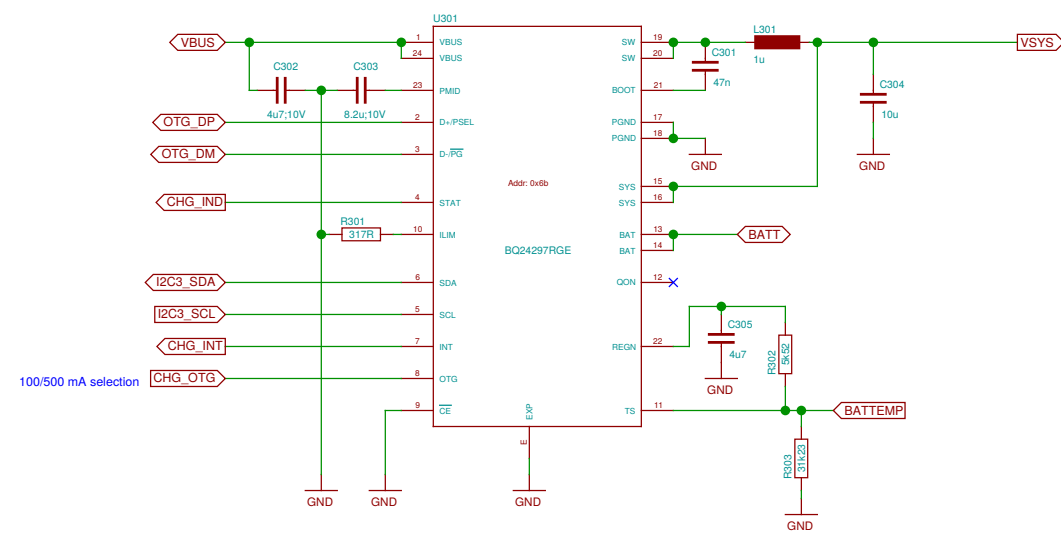
Note regarding I2C addresses:
Addresses in the schematics are provided for convenience.
The authoritative source is
<https://neo900.org/git?p=misc;a=tree;f=i2c>

Sheet: /	
File: neo900.sch	
Title: Neo900	
Size: A3	Date: 16 JUL 2016
Plotted by eeshow 2f031f5+ 20161019-02:26Z	
Rev:	Id: 1/37

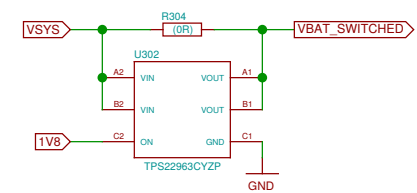


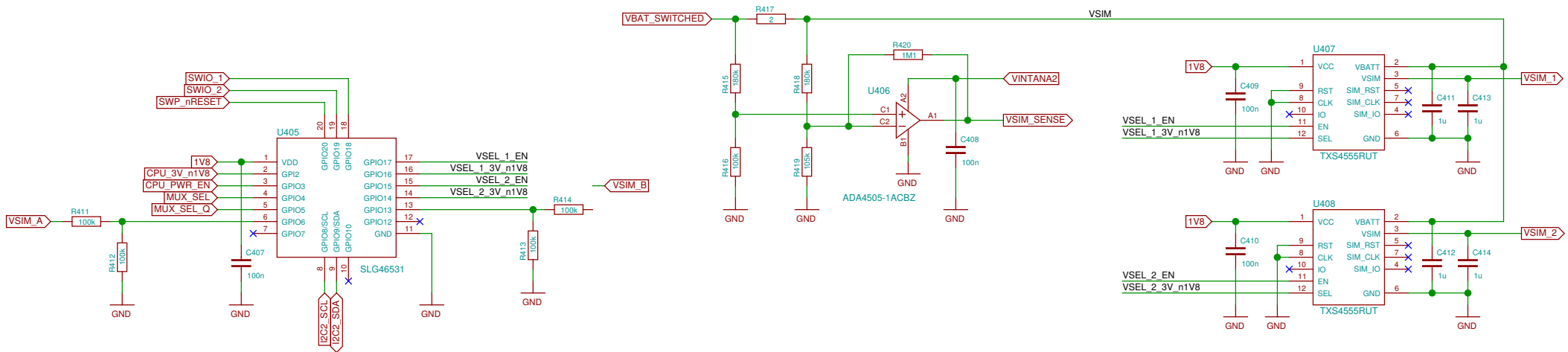
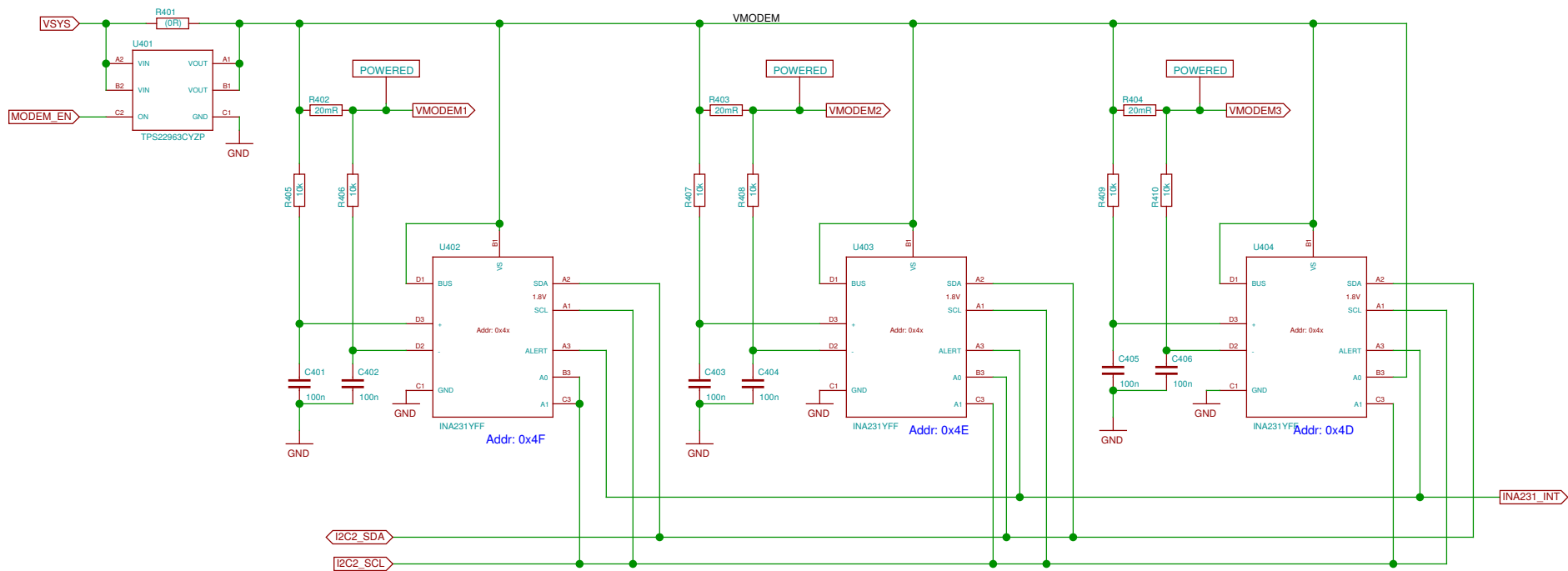
place in scan matrix? would need 3-4 wires to UPPER board instead of 2

in any case it is sufficient to connect GPIO-VOL+ and VOL- to two pins on the B2B connector

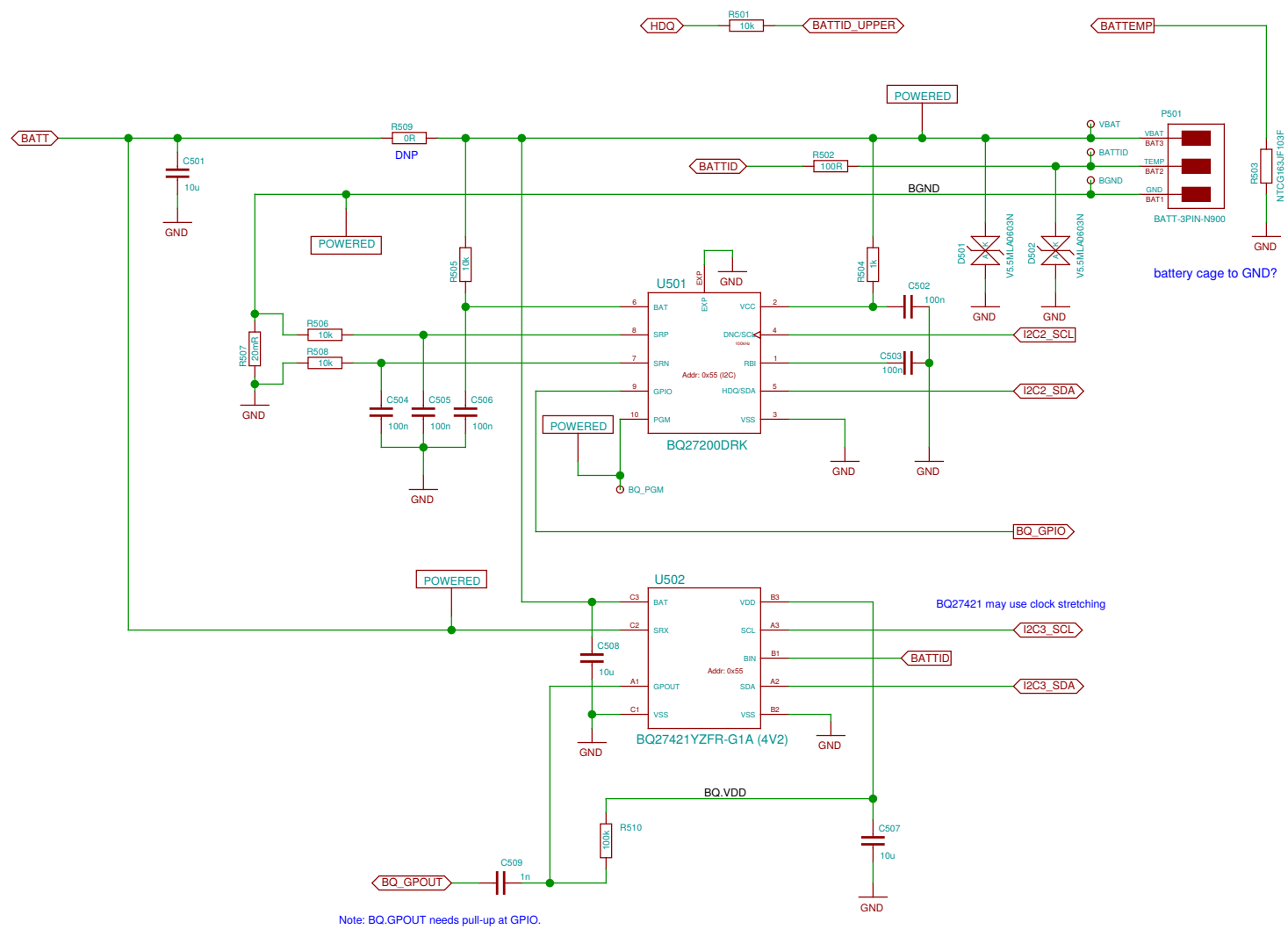


100/500 mA selection





TODO: update SLG design for changed pins

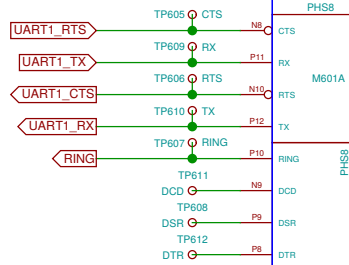
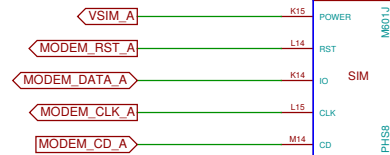
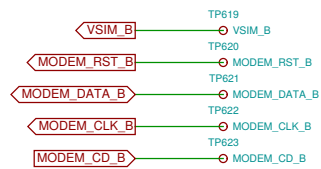
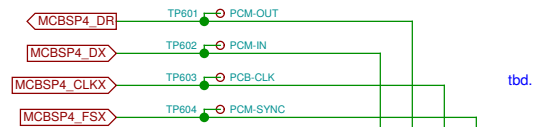
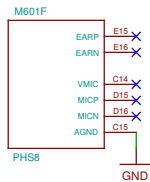


battery cage to GND?

BQ27421 may use clock stretching

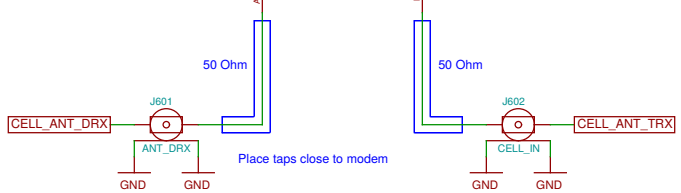
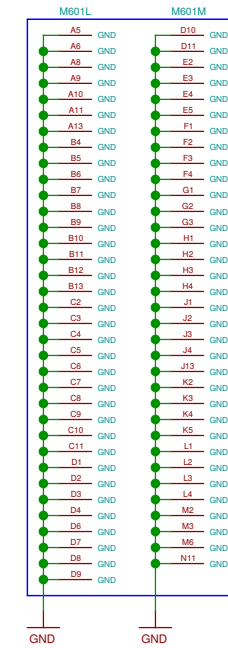
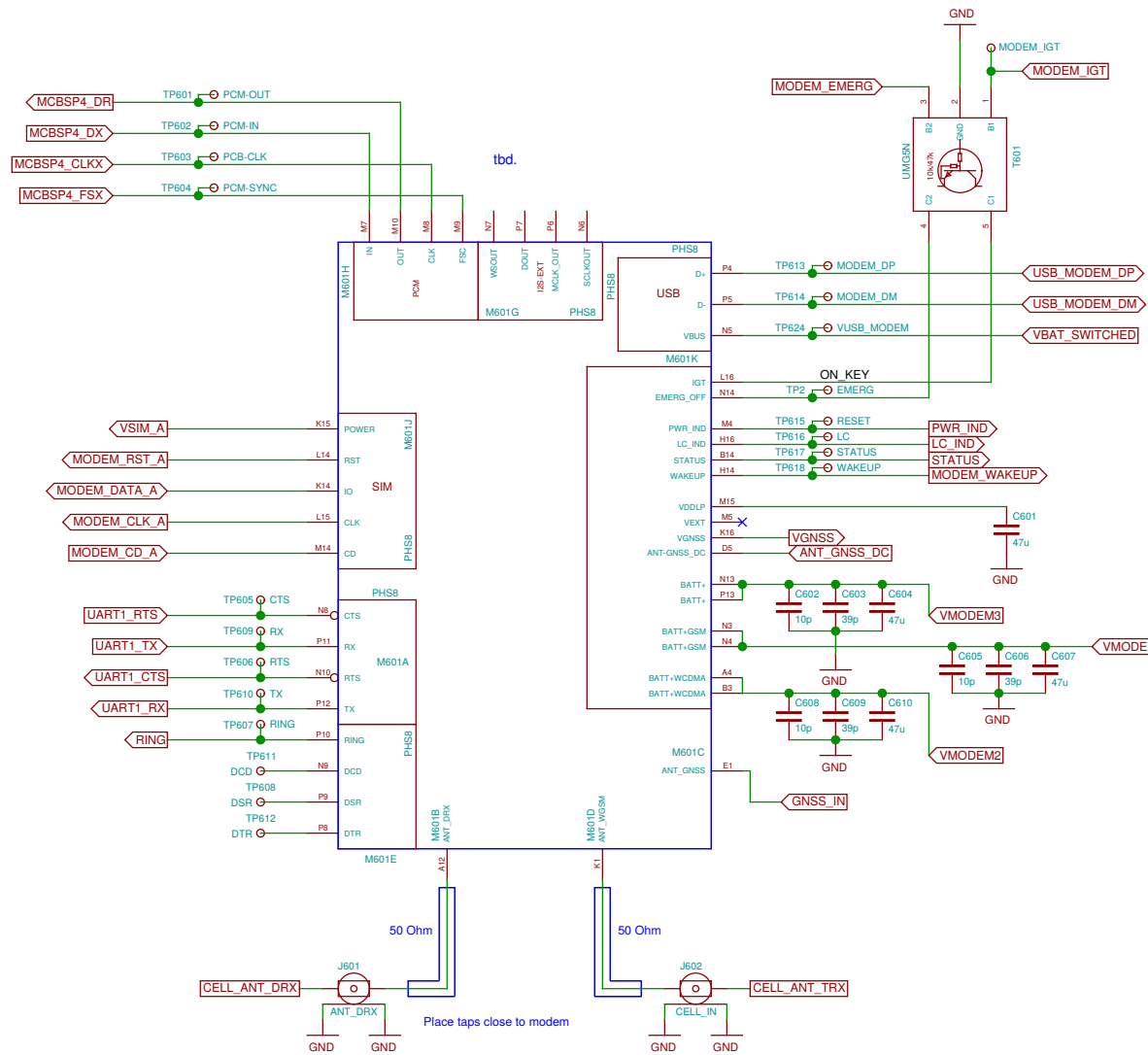
Note: BQ.GPOUT needs pull-up at GPIO.

Sheet: /Fuel Gauge/		Date: 17 JUL 2016	
File: neo900_SS_5.sch		Rev:	
Title: Fuel Gauge			
Size: A3	Plotted by eeshow 2f031f5+ 20161019-02:26Z	Id: 5/37	



TODO: B-SIM bus FFS

Can we connect UART in parallel to Bluetooth UART (i.e. if BT is disabled we can unbrick the Modem?)



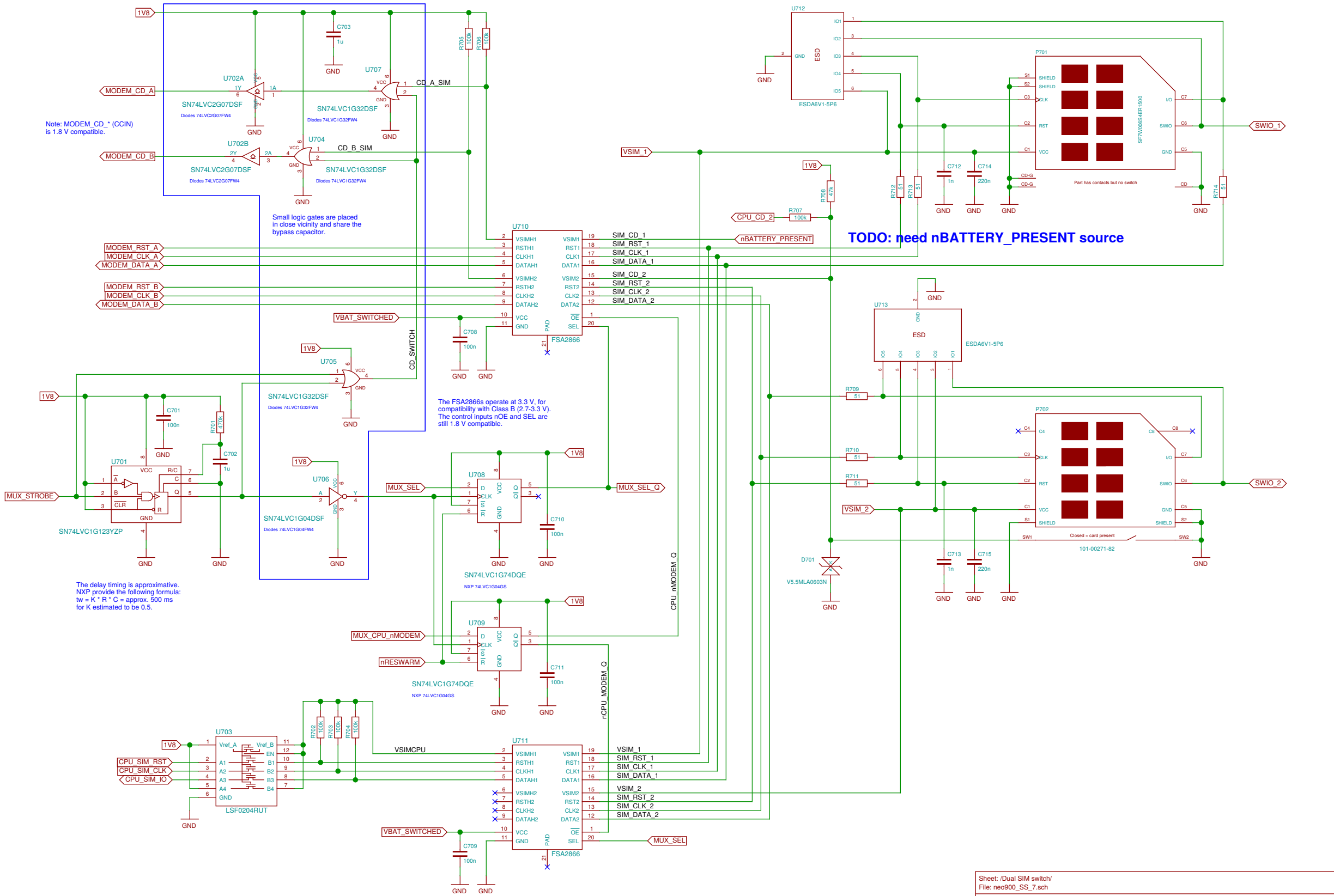
Note: MODEM_CD_* (CCIN) is 1.8 V compatible.

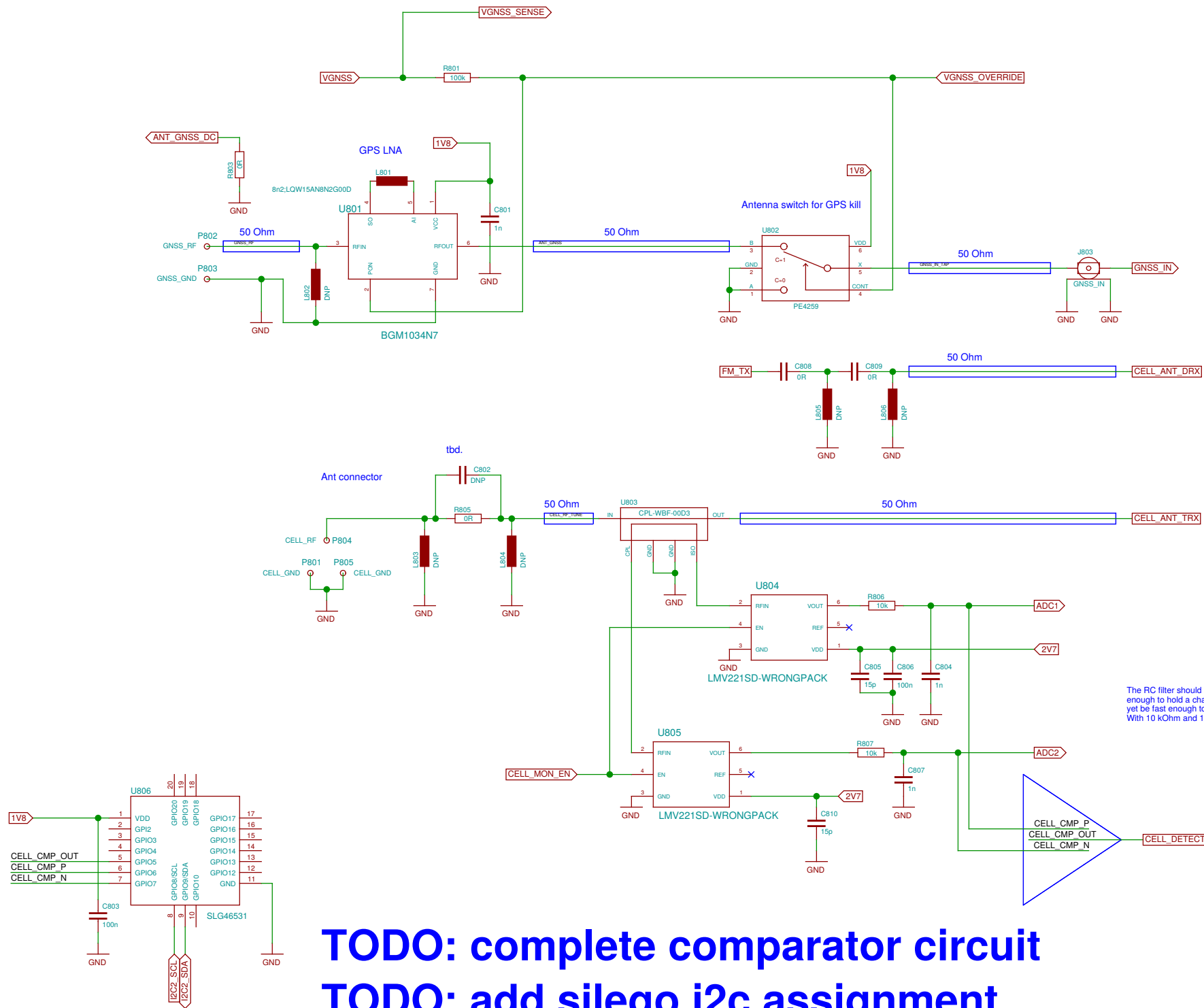
Small logic gates are placed in close vicinity and share the bypass capacitor.

The FSA2866s operate at 3.3 V, for compatibility with Class B (2.7-3.3 V). The control inputs nOE and SEL are still 1.8 V compatible.

The delay timing is approximative. NXP provide the following formula: $t_w = K * R * C = \text{approx. } 500 \text{ ms}$ for K estimated to be 0.5.

TODO: need nBATTERY_PRESENT source

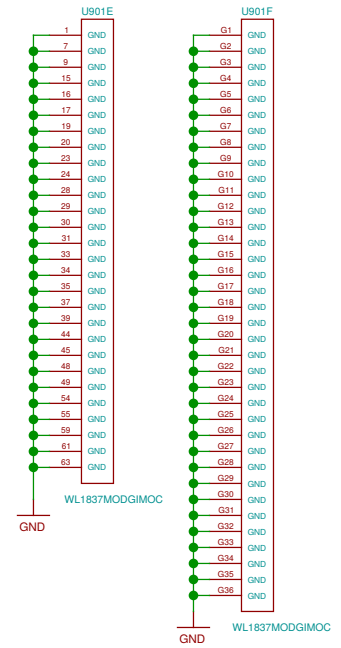
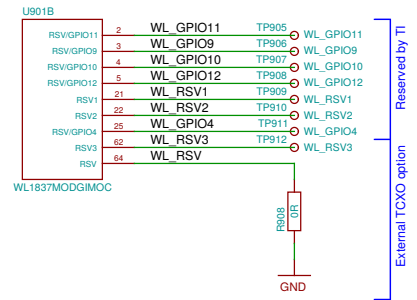
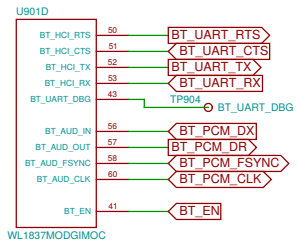
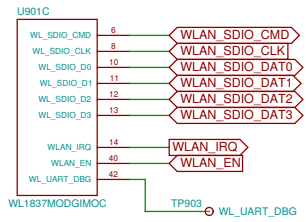
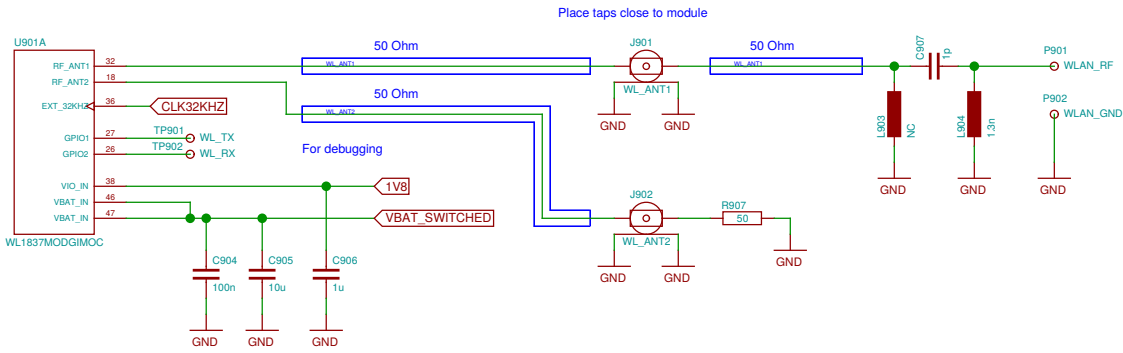




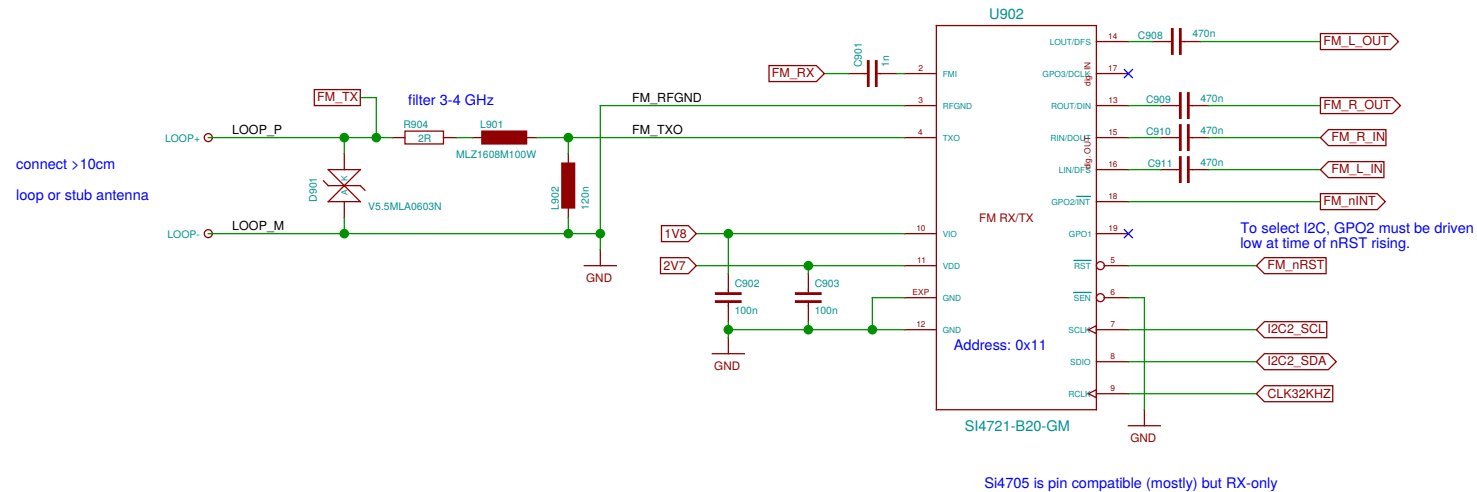
The RC filter should have C large enough enough to hold a charge in pulsed operation, yet be fast enough to detect short activity. With 10 kOhm and 1 nF, we get about 16 kHz.

TODO: complete comparator circuit
TODO: add silego i2c assignment
TODO: iox

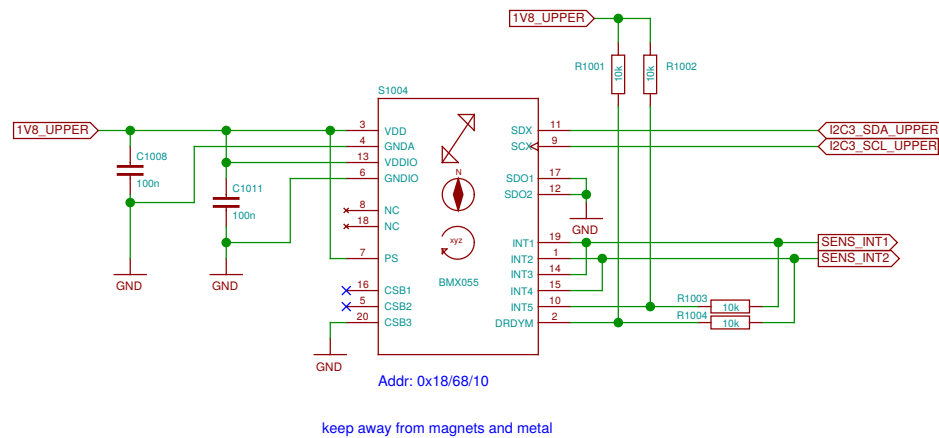
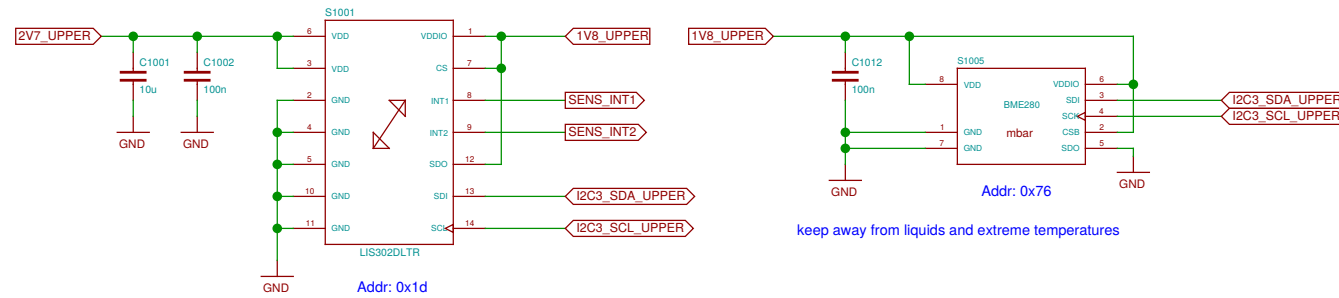
TODO: assign footprints



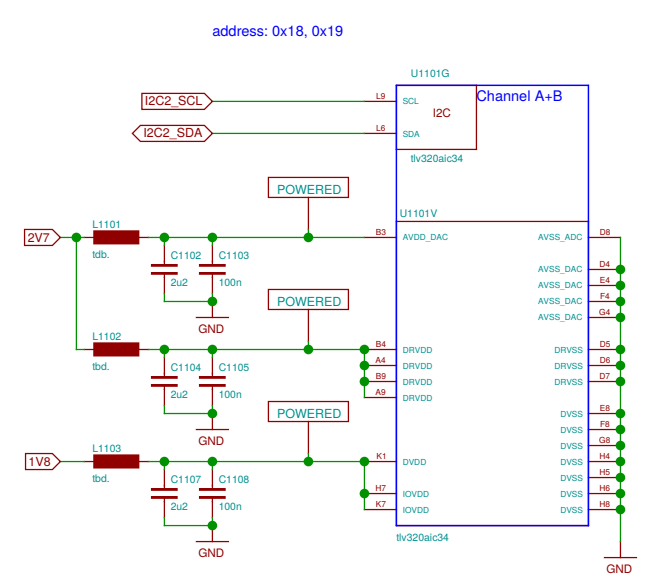
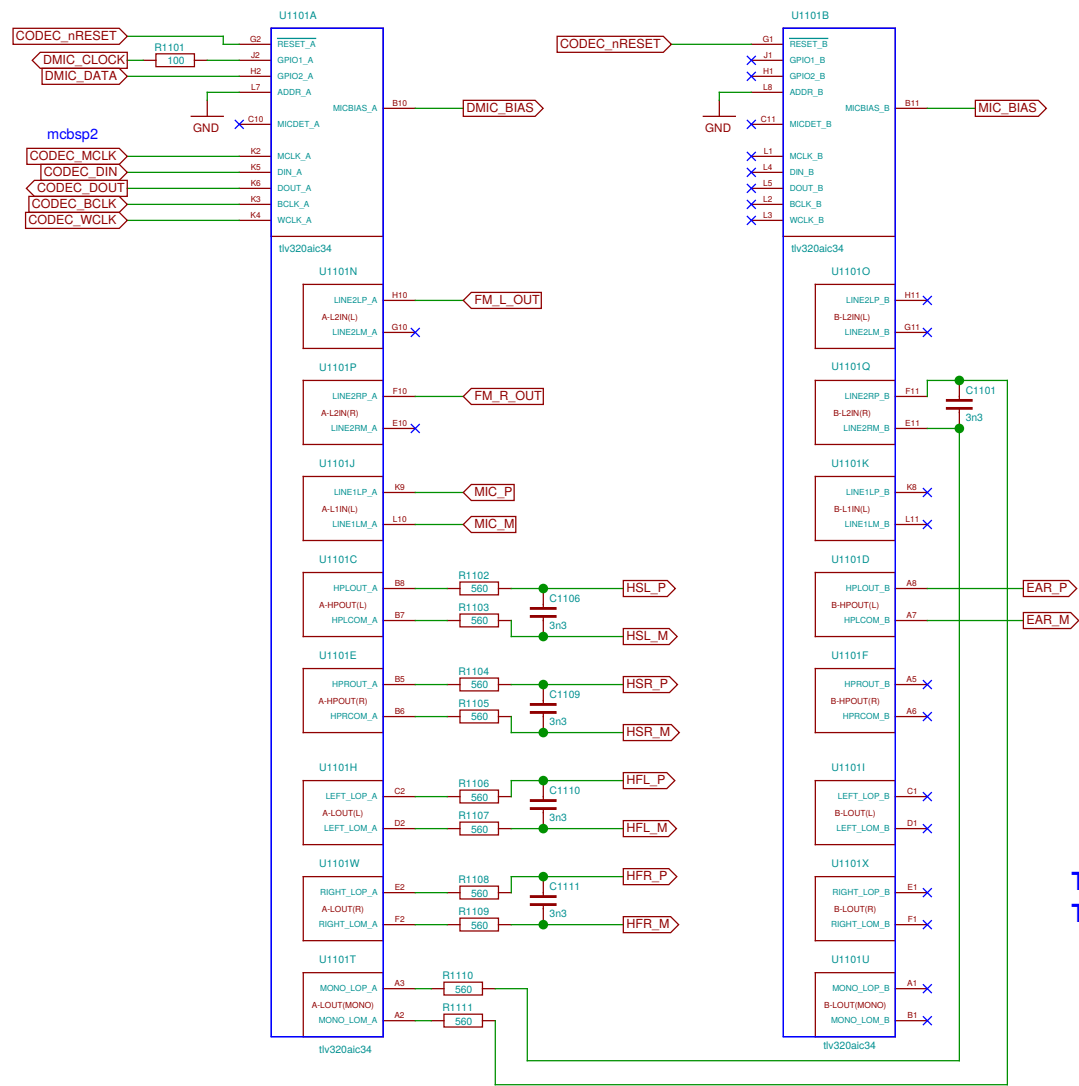
TODO: check caps



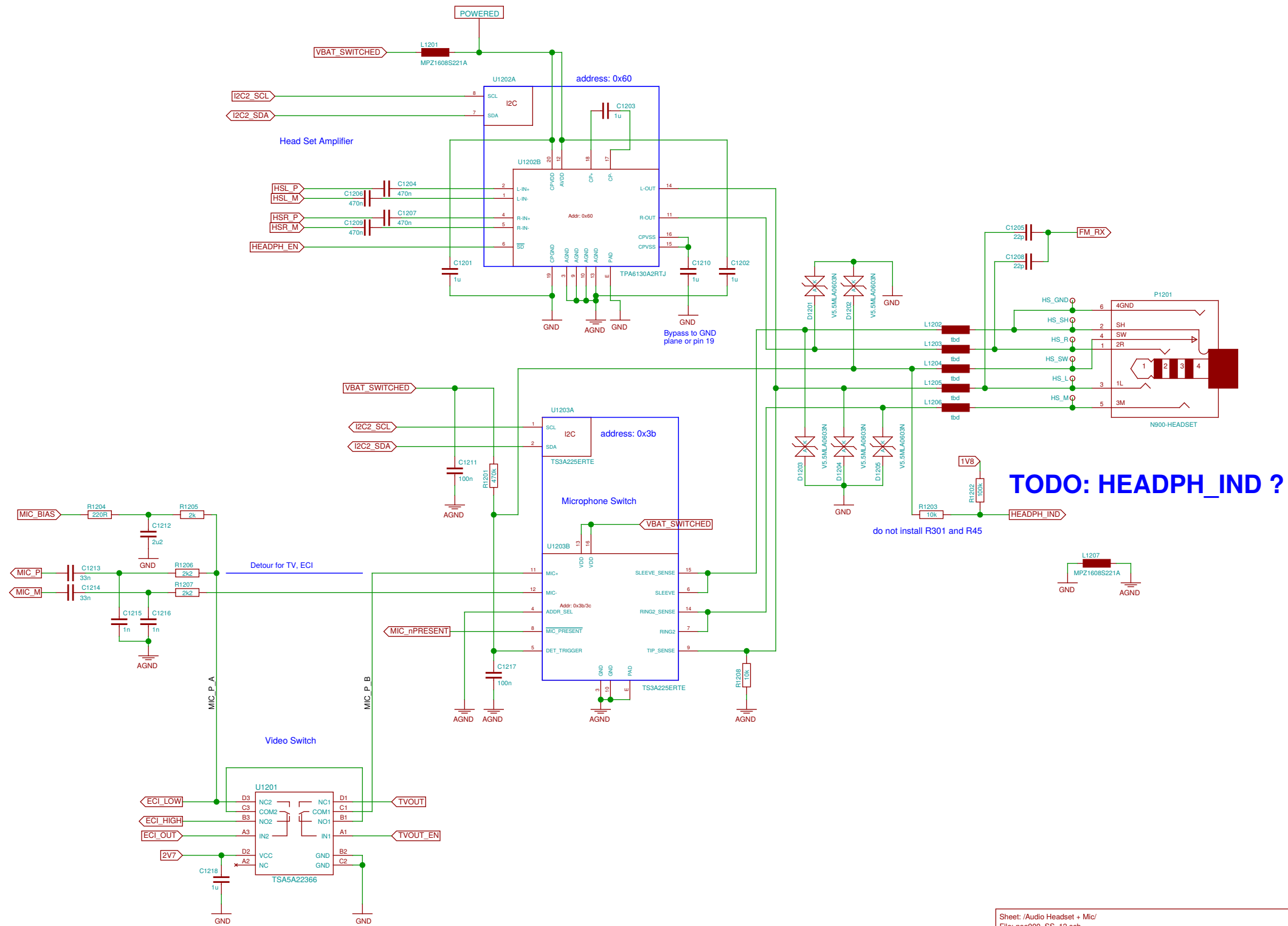
Si4705 is pin compatible (mostly) but RX-only



problem: this is a 0.5mm BGA making lower board expensive
 but it appears to be not extremely critical (only 3 rows and inner ring is GND)
 problem: analog mic is on upper board
 alternative: place on upper board (to be evaluated)

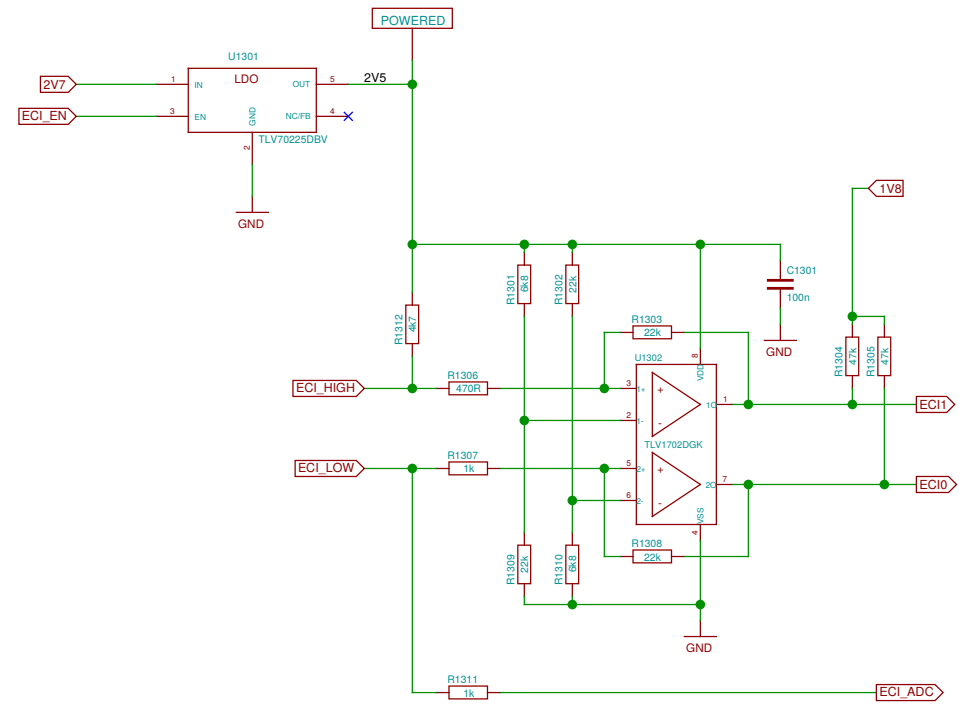


TODO: assign FM out (FM_L_IN, FM_R_IN)
 TODO: IR_AUDIOIN

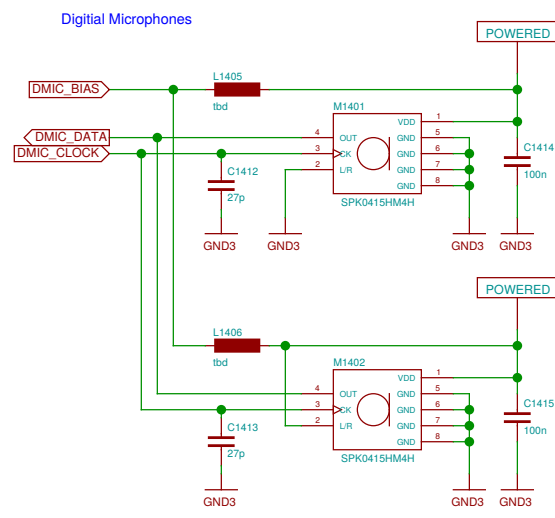
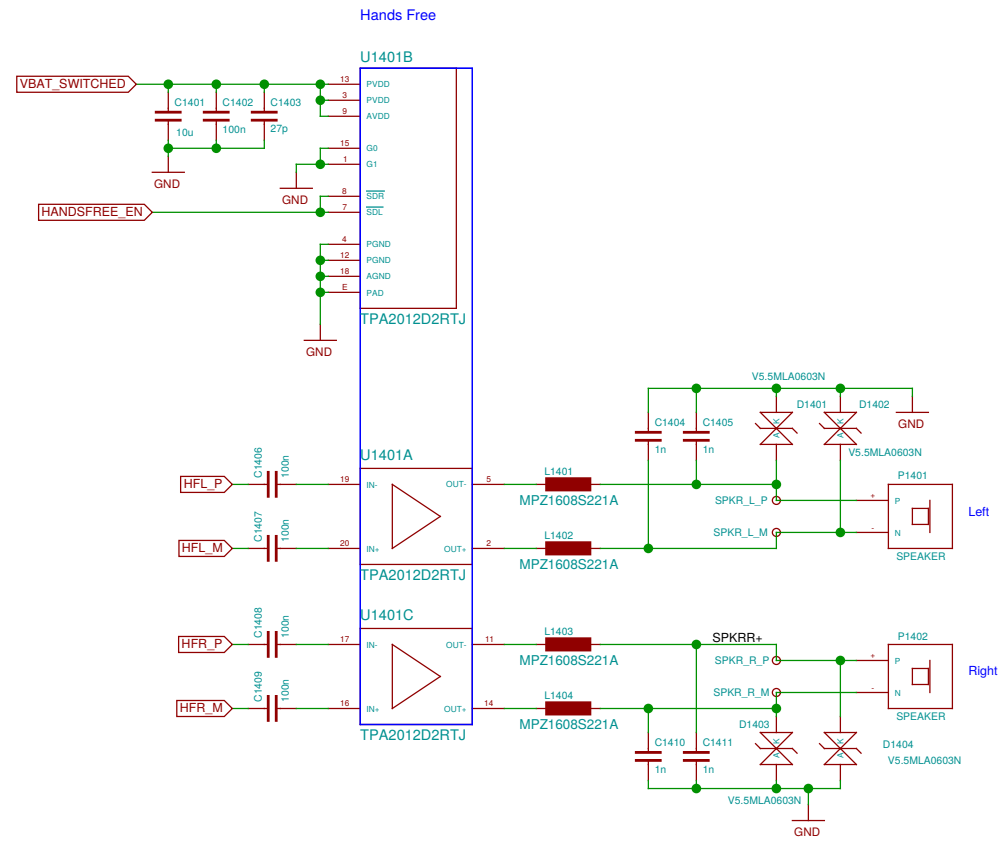


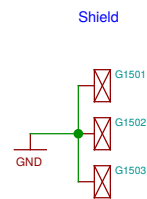
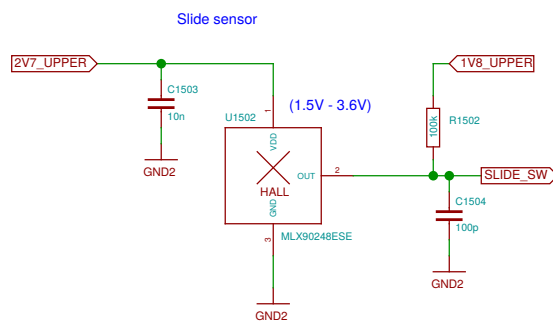
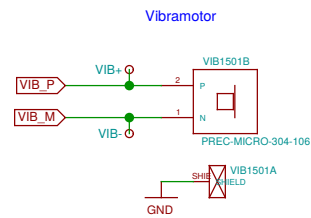
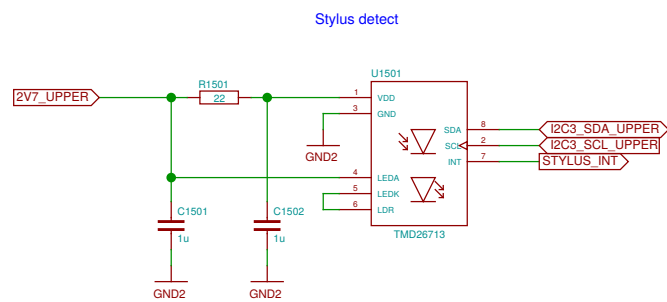
TODO: HEADPH_IND ?

do not install R301 and R45

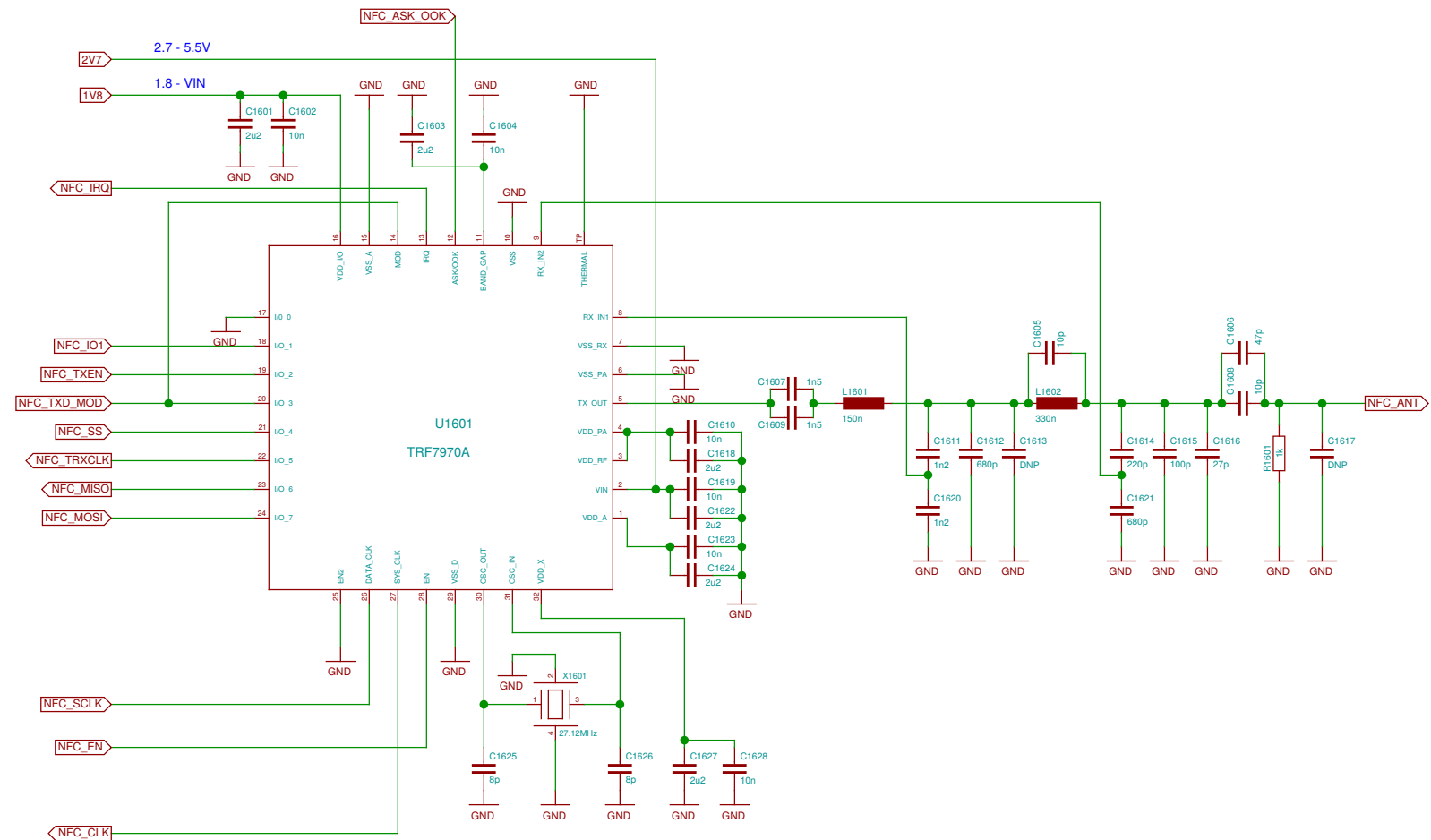


Sheet: /ECI/		File: neo900_SS_13.sch	
Title: ECI			
Size: A3	Date: 17 JUL 2016	Rev:	
Plotted by eeshow 2103115+ 20161019-02:26Z		Id: 13/37	

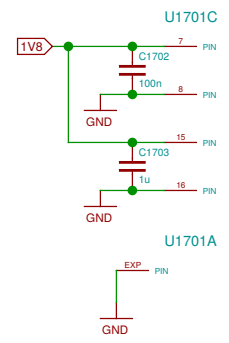
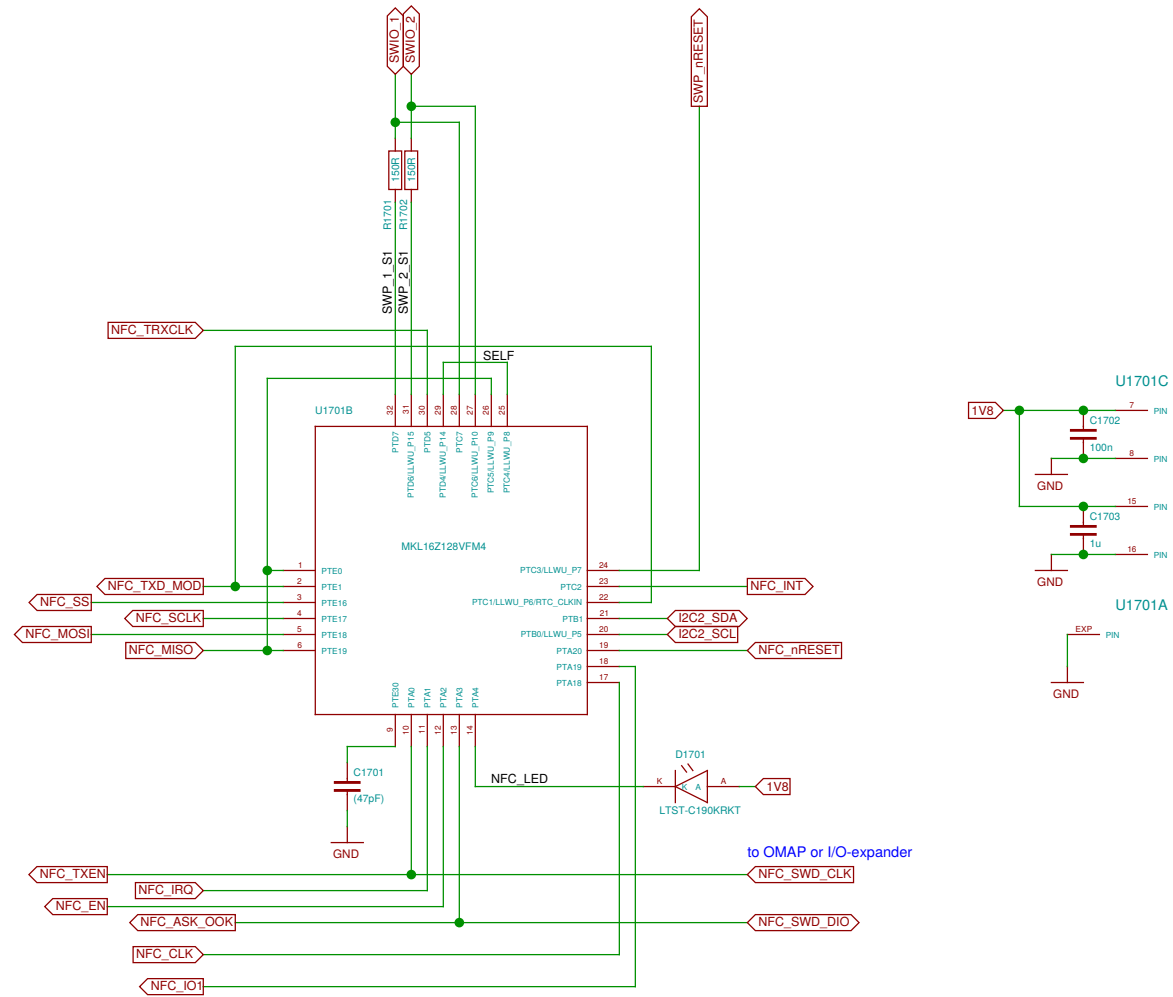




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Size: A3	Date: 17 JUL 2016
Plotted by eeshow 2f031f5+ 20161019-02:26Z	
Rev:	Id: 15/37

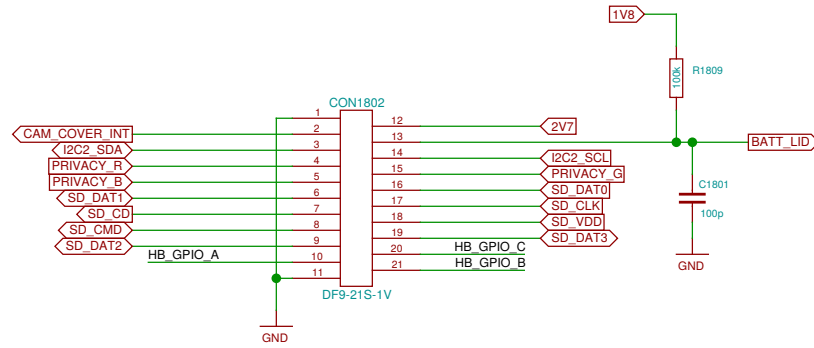
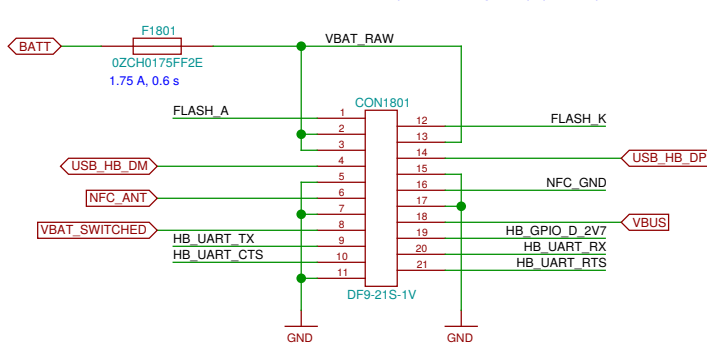


Some choices, 3.2 x 2.6 mm, 8-10 pF:
 NDK NX3225GA-27.12M-STD-CRG-2
 NDK NX3225SA-27.12M-STD-CSR-3
 Tattien XXCCEINANF-27.120000

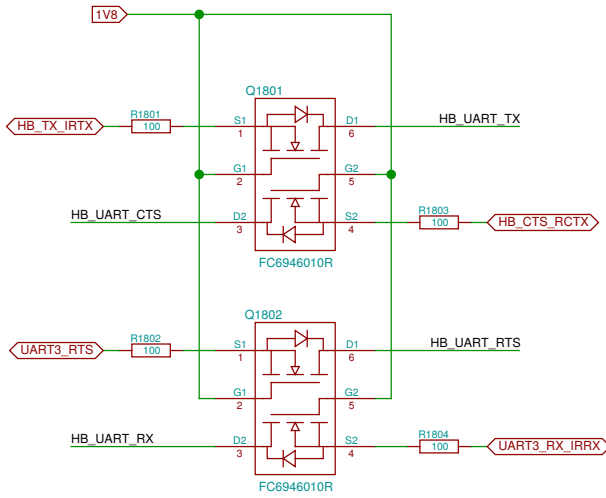
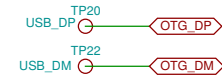


The LOWER-BOB interconnect is defined in the Hackerbus specification
<http://neo900.org/stuff/papers/hb.pdf>

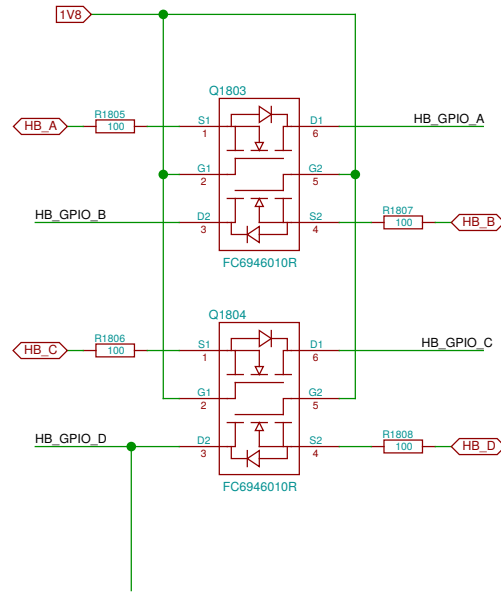
NOTE: this is mangling up Breakout and Lower board connectors
 Signals may have to be fed through the breakout board connector increasing resistance



TODO: define NFC-GND

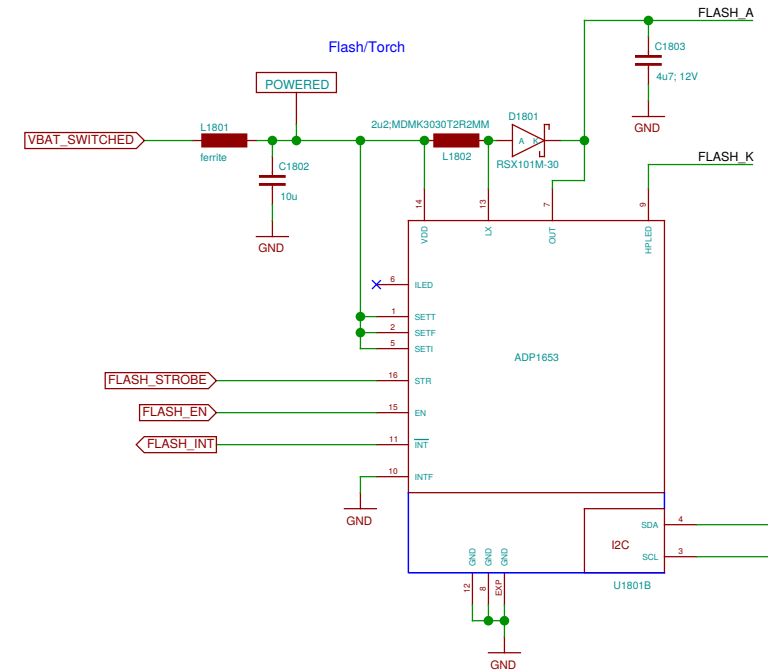


Q18xx alternative: Diodes DMN63D8LV



TODO: 2V7+SW / LDO ?

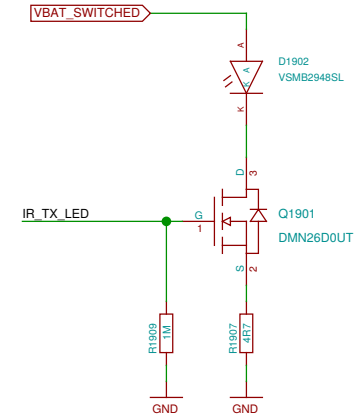
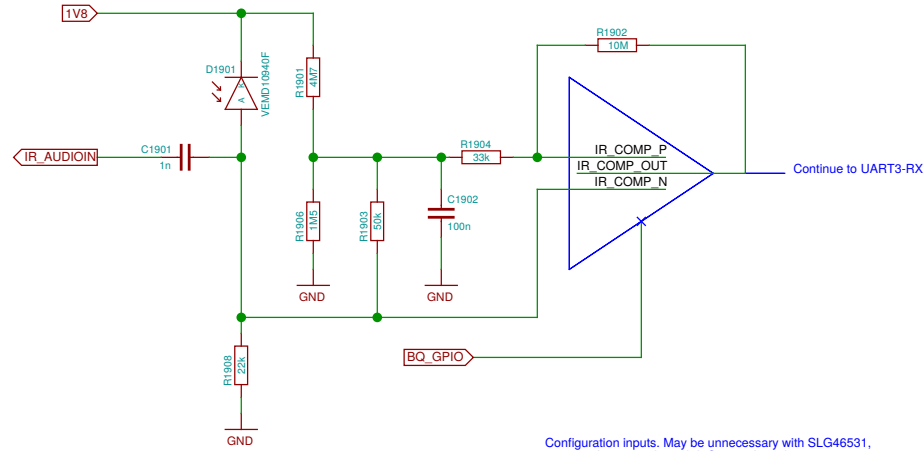
Missing 6x 2R for alternate function select (do we have the space for ca. 2.5 x 5mm?)



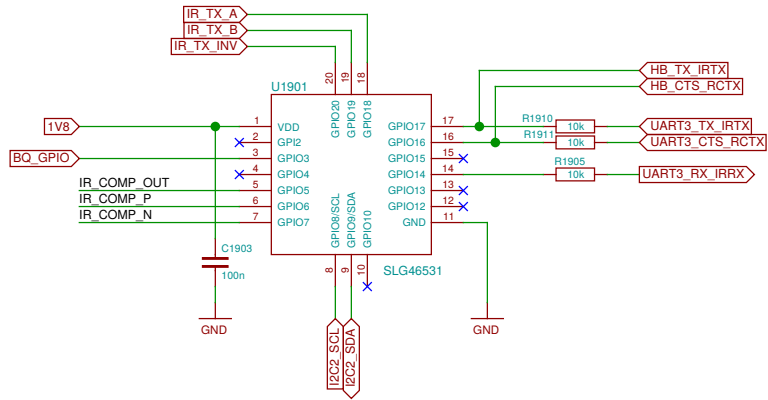
TODO: HB USB PHY may go here

TODO: update D1901 footprint

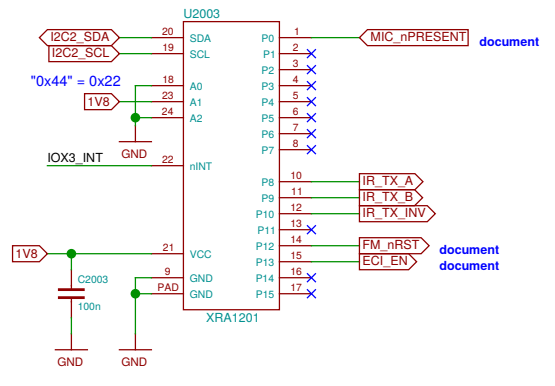
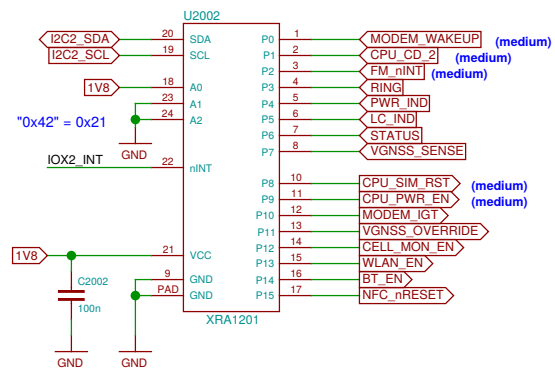
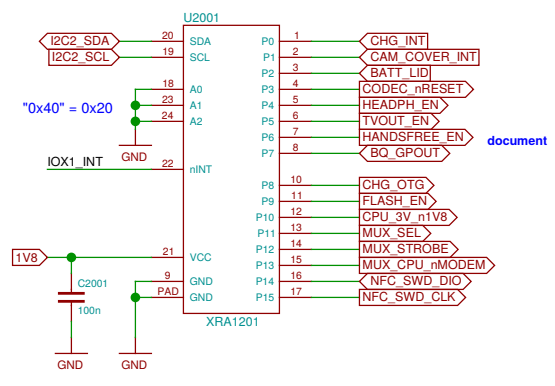
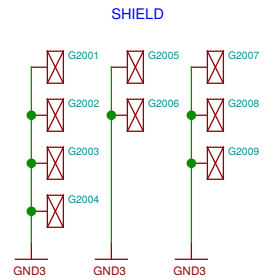
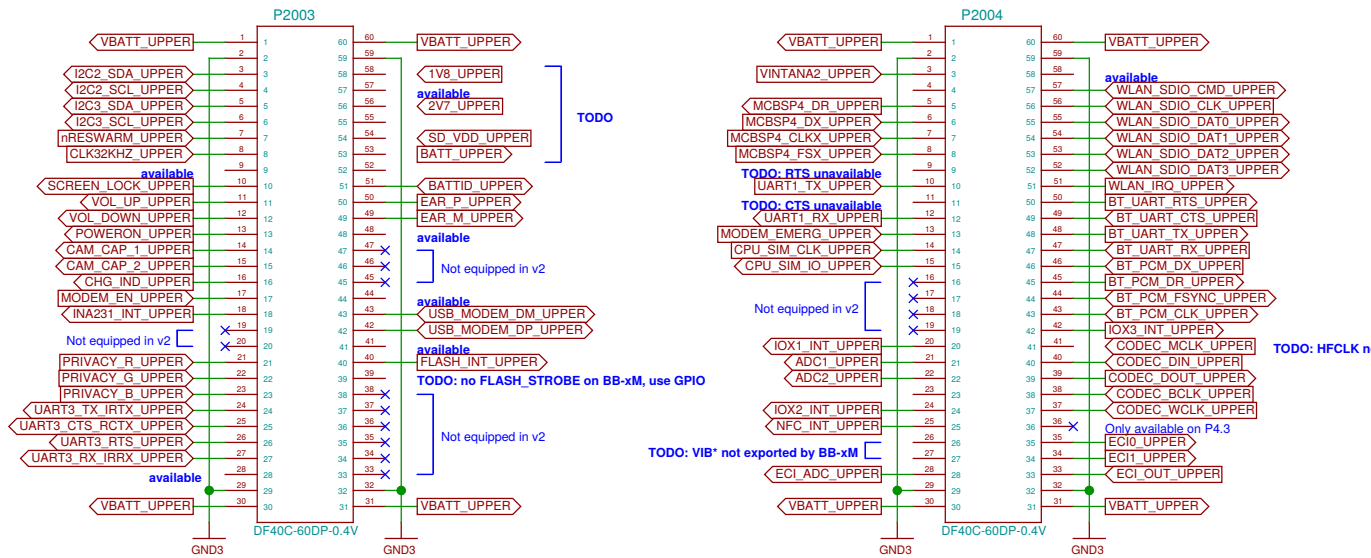
NOTE: 1V8 may be quite noisy



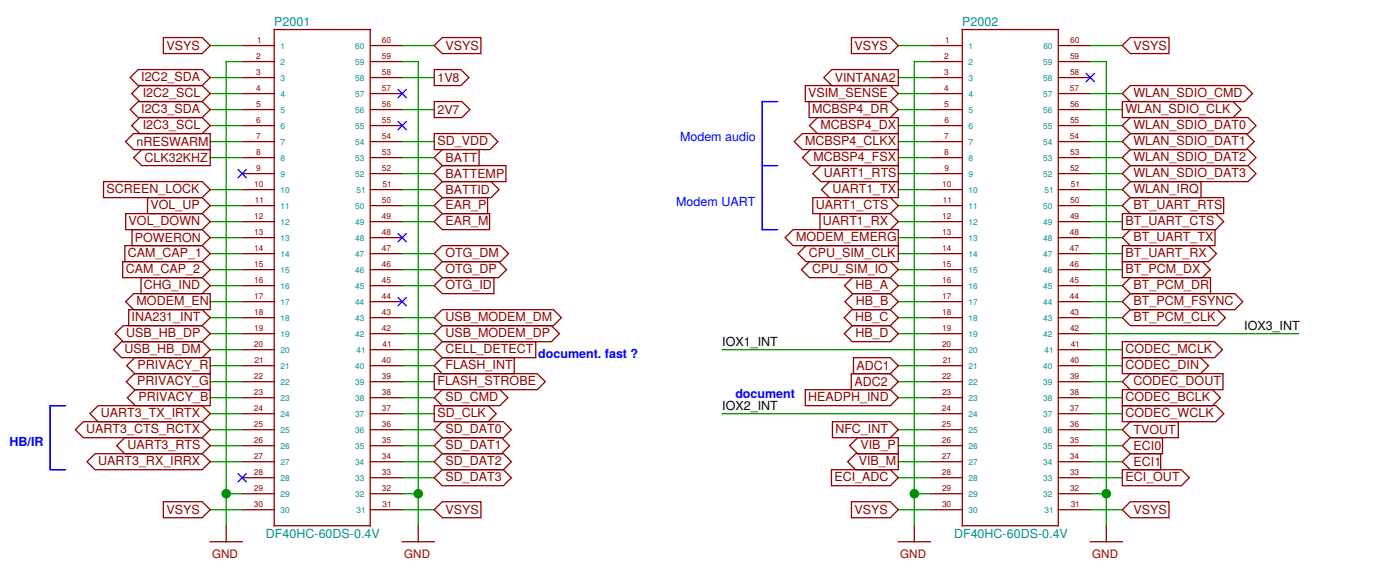
Configuration inputs. May be unnecessary with SLG46531, once configuration through I2C is confirmed.



This is just the collection of signals we have. Proper assignment still pending.

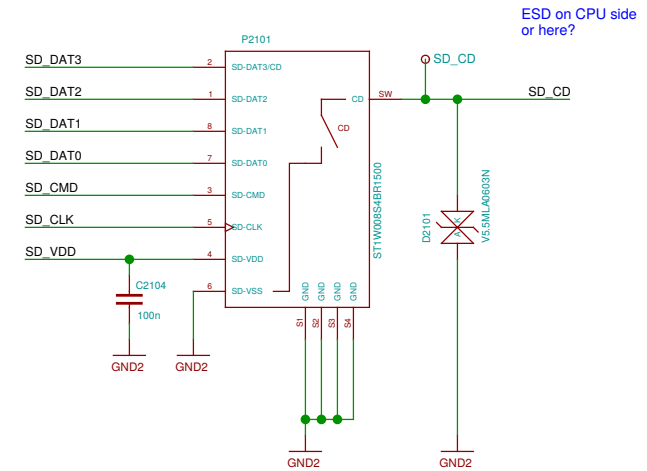
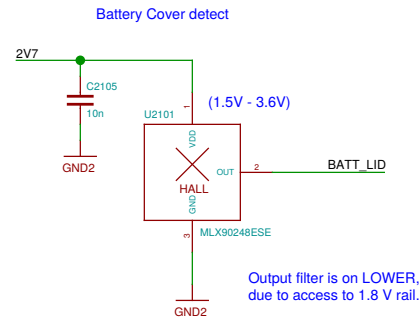
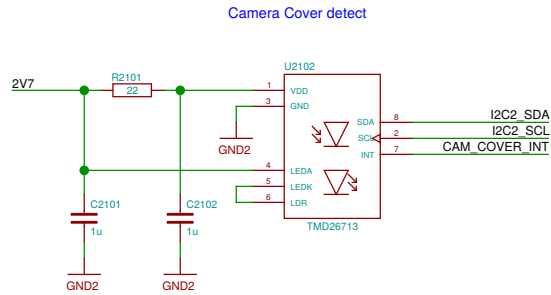


UPPER
LOWER

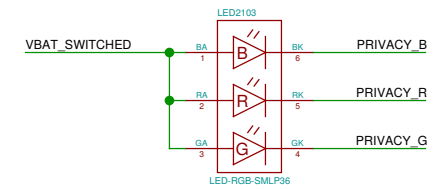
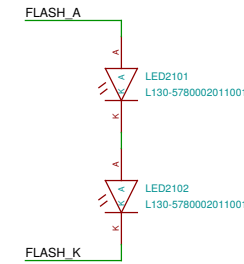
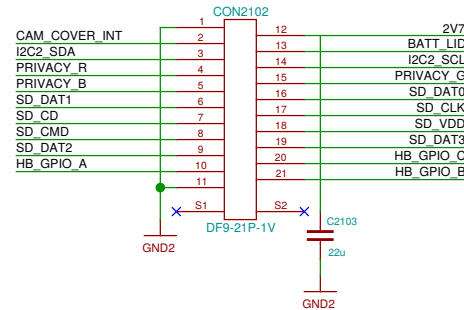
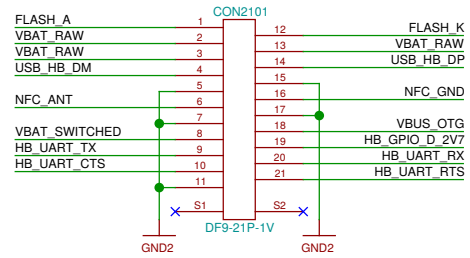


Current rating per contact: 0.3 A

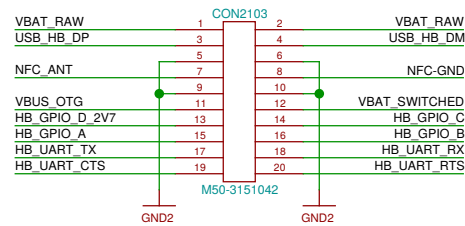
TODO: add ESD protection (here)



The LOWER_BOB interconnect is defined in the Hackerbus specification
<http://neo900.org/stuff/papers/hb.pdf>



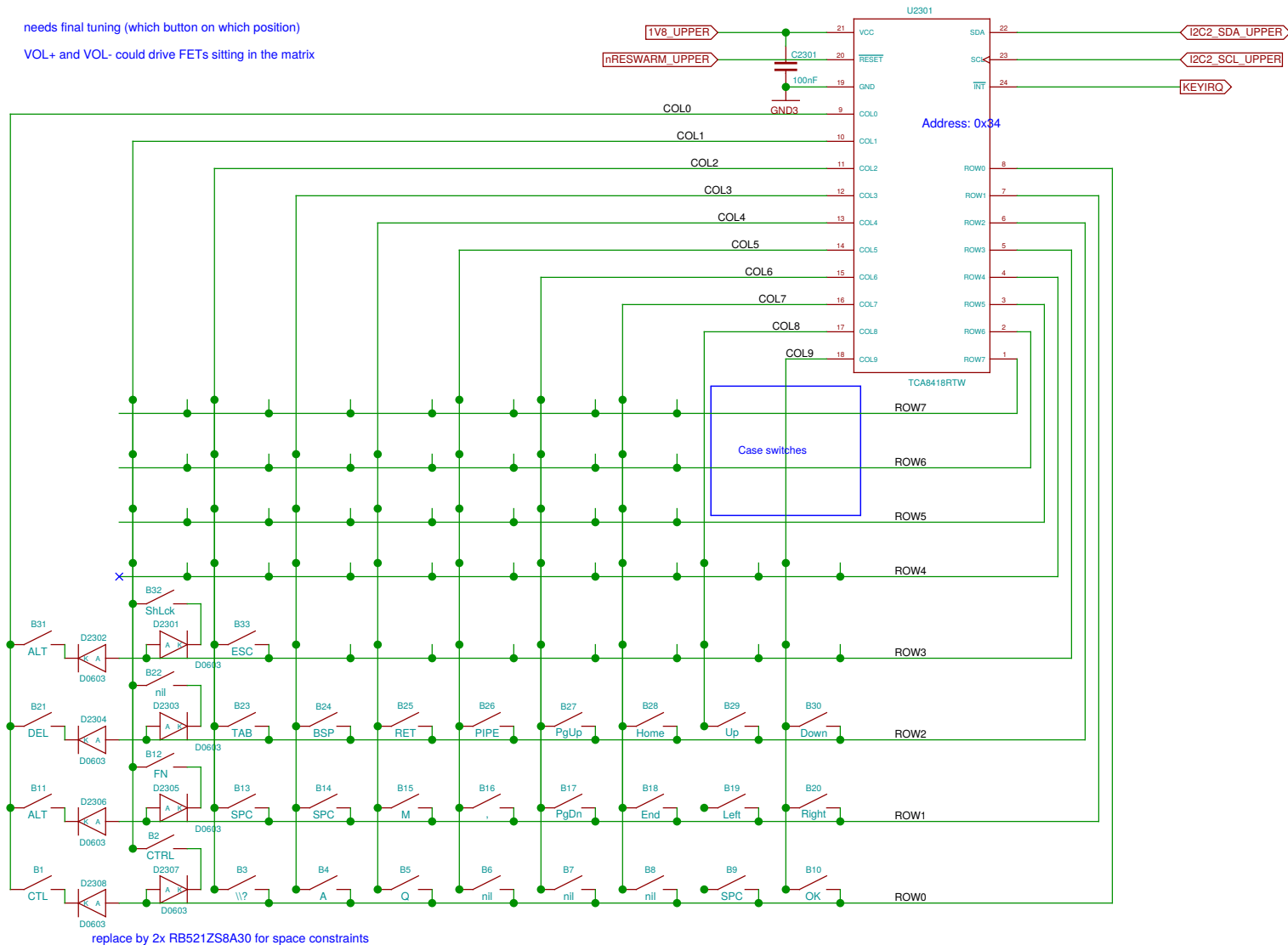
Hackerbus



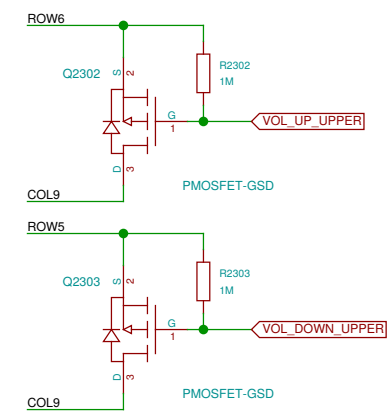
TODO: consider sheet for deletion

Sheet: /empty/ File: neo900_SS_22.sch		
Title: empty		
Size: A3	Date: 17 JUL 2016	Rev:
Plotted by eeshow 2103115- 20161019-02:26Z		Id: 22/37

needs final tuning (which button on which position)
 VOL+ and VOL- could drive FETs sitting in the matrix



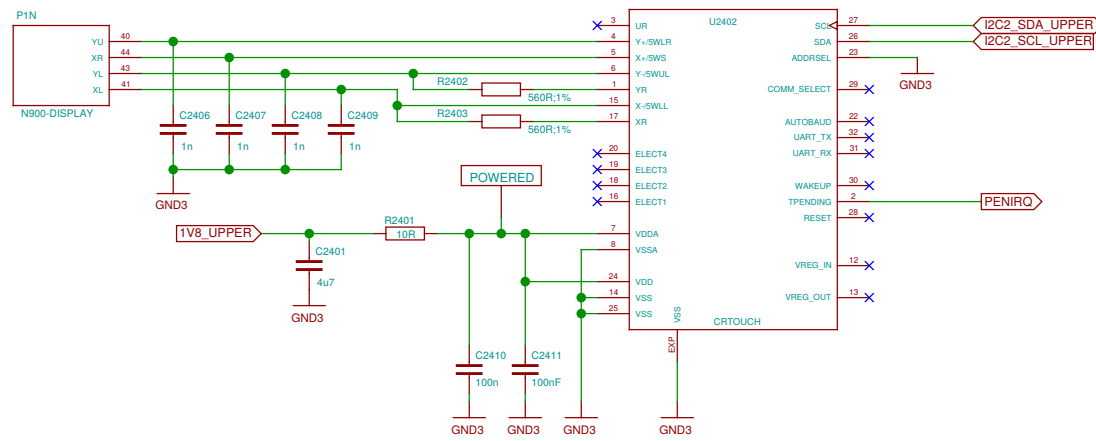
replace by 2x RB521ZS8A30 for space constraints



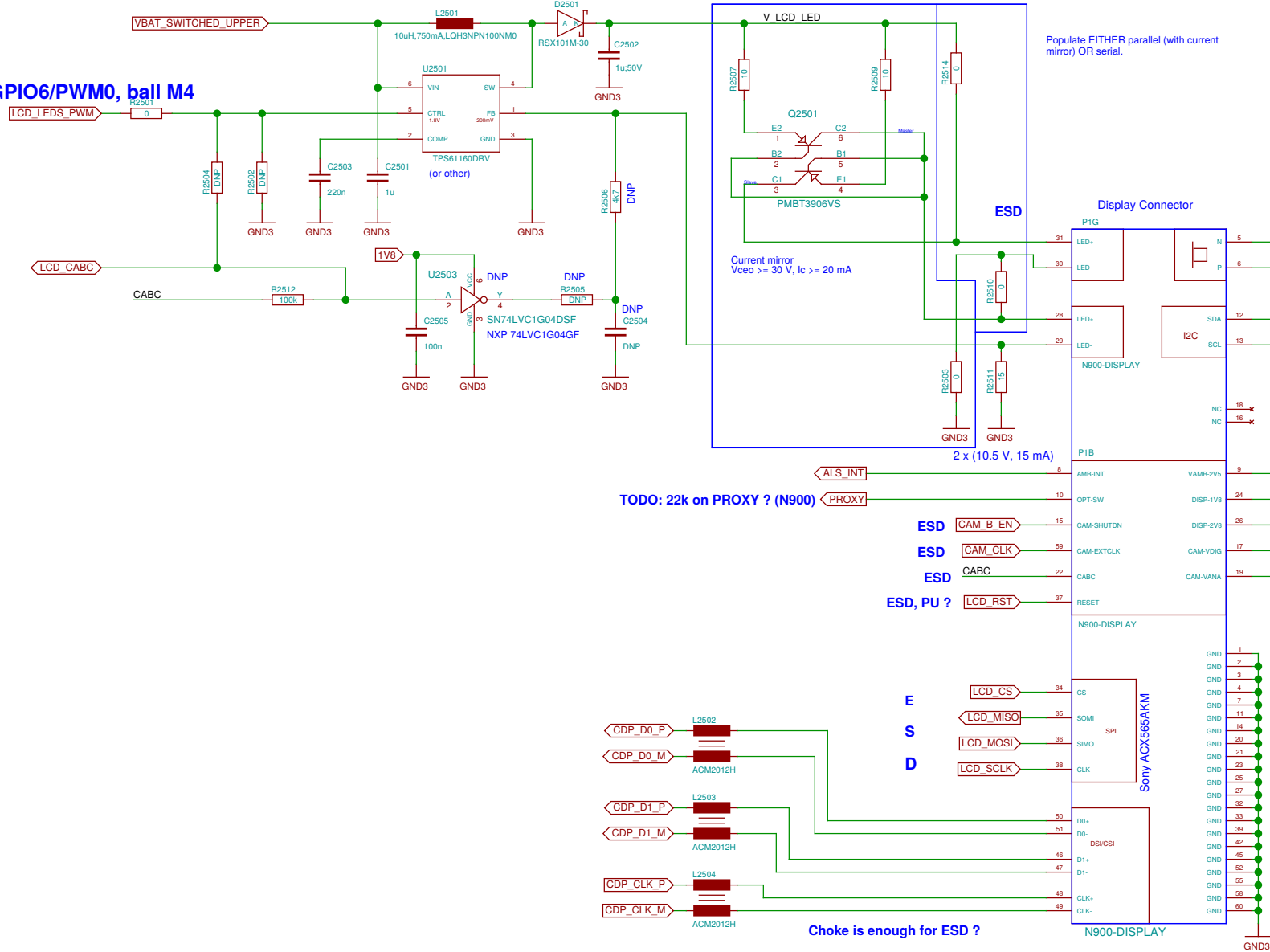
TODO: key names are nonsense

TODO: rearrange matrix to avoid diodes ?

Resistive Touch (display connector)



TWL4030, GPIO6/PWM0, ball M4



OMAP is not part of v2

Sheet: /CPU + PoP RAM/NAND/		
File: neo900_SS_26.sch		
Title: CPU + PoP RAM/NAND		
Size: A3	Date: 17 JUL 2016	Rev:
Plotted by eeshow 2103115+ 20161019-02:26Z		Id: 26/37

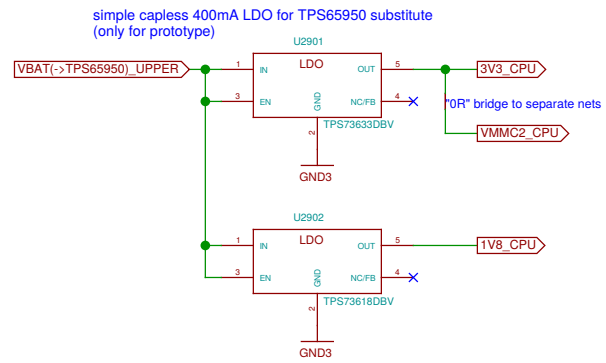
eMMC is not part of v2

Sheet: /eMMC/ File: neo900_SS_27.sch		
Title: eMMC		
Size: A3	Date: 17 JUL 2016	Rev:
Plotted by eeshow 2103115+ 20161019-02:26Z		Id: 27/37

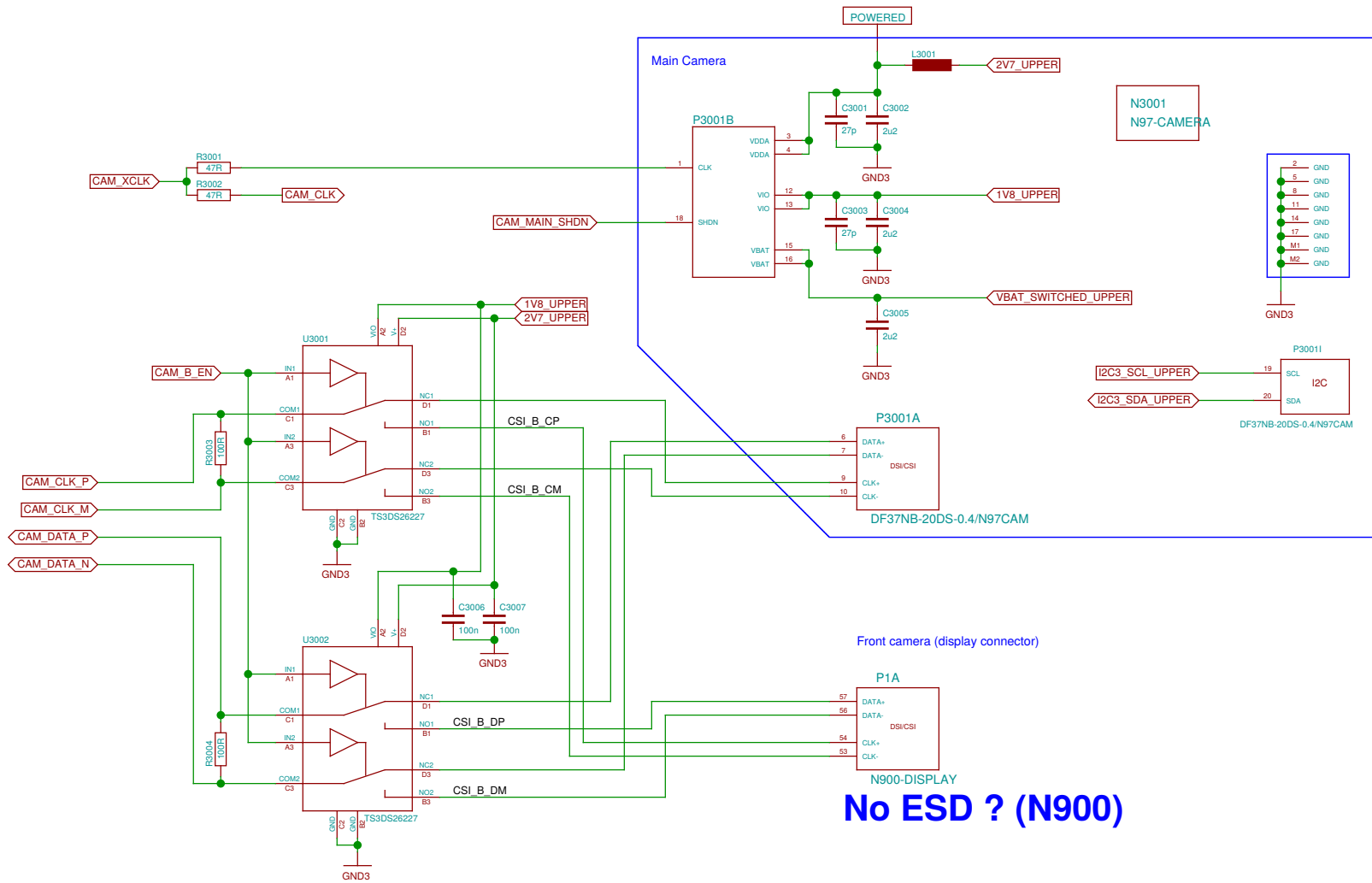
Companion chip (TPS65950) is not part of v2

Sheet: /PMU+Codec/ File: neo900_SS_28.sch		
Title: PMU+Codec		
Size: A3	Date: 17 JUL 2016	Rev:
Plotted by eeshow 2103115+ 20161019-02:26Z		Id: 28/37

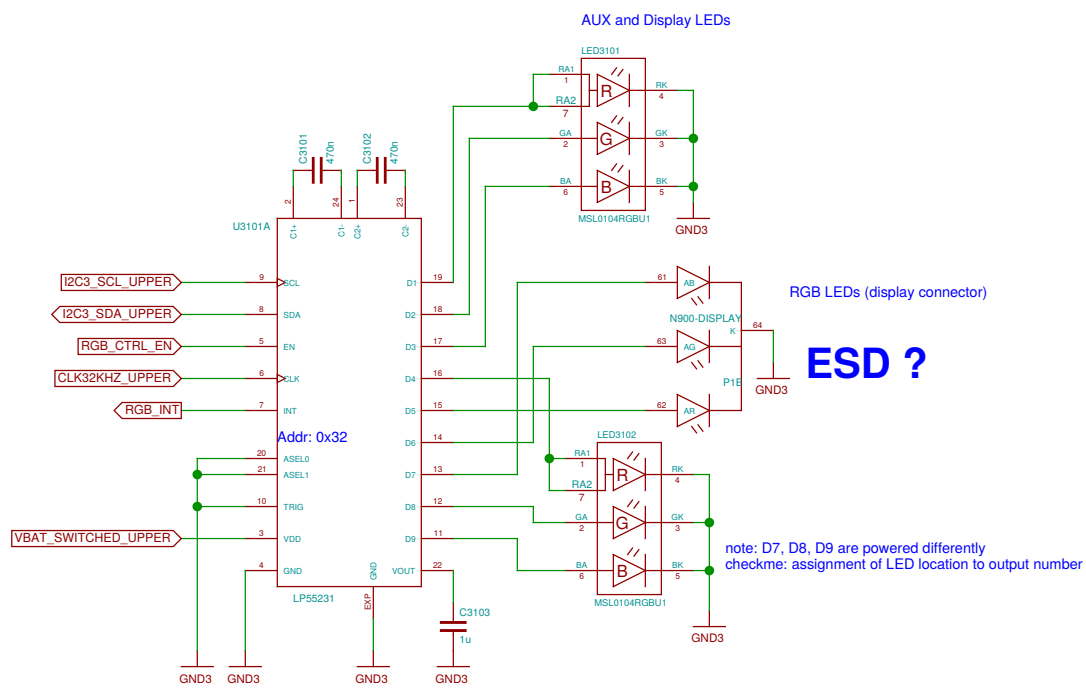
TODO: empty this sheet, too ?



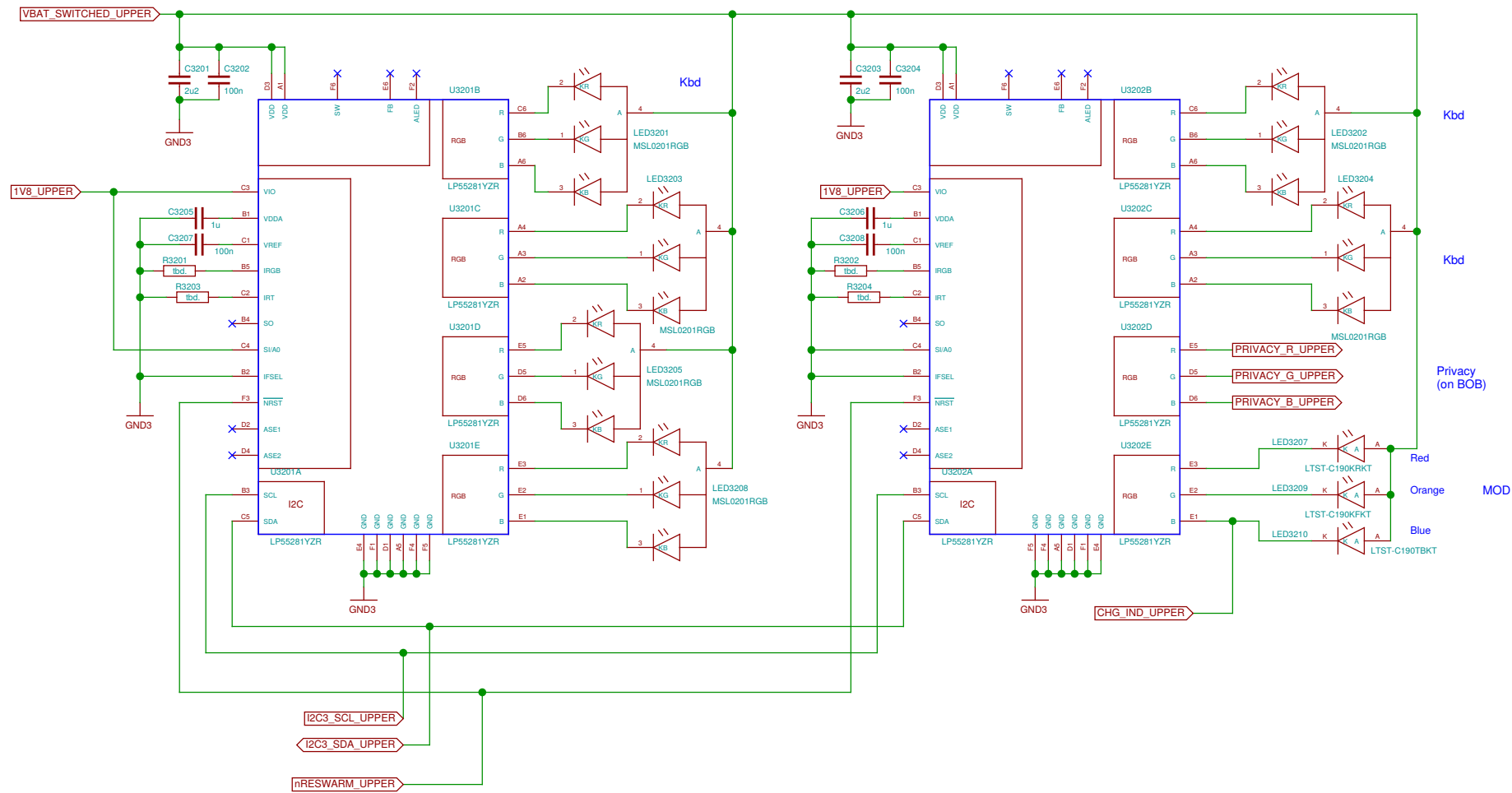
Sheet: /BB-XM Dummy (TWL4030)/	
File: neo900_SS_29.sch	
Title: BB-XM Dummy (TWL4030)	
Size: A3	Date: 17 JUL 2016
Plotted by: eeshow 2f031f5+ 20161019-02:26Z	Rev:
	Id: 29/37



Sheet: /Camera/ File: neo900_SS_30.sch	
Title: Camera	
Size: A3	Date: 17 JUL 2016
Plotted by eeshow 2f031f5 - 20161019-02:26Z	
Rev:	Id: 30/37

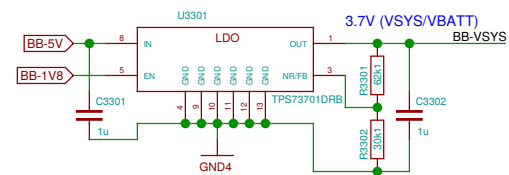


Sheet: /Fancy LEDs/		
File: neo900_SS_31.sch		
Title: Fancy LEDs		
Size: A3	Date: 17 JUL 2016	Rev:
Plotted by eeshow 2/03/15+ 2016/10/19-02:26Z		Id: 31/37



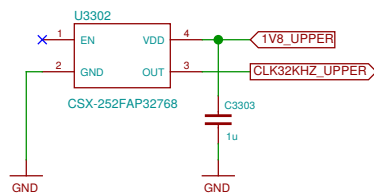
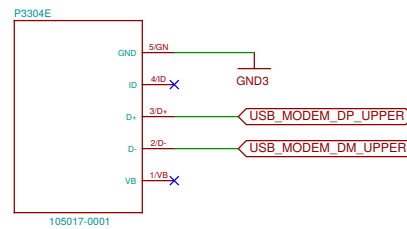
Cleaning up. The connections to BB-xM are on the next sheets.

TODO: v2 power supply still needs designing



Ersetzen durch 2A buck converter

connect to BB by some Micro-USB cable

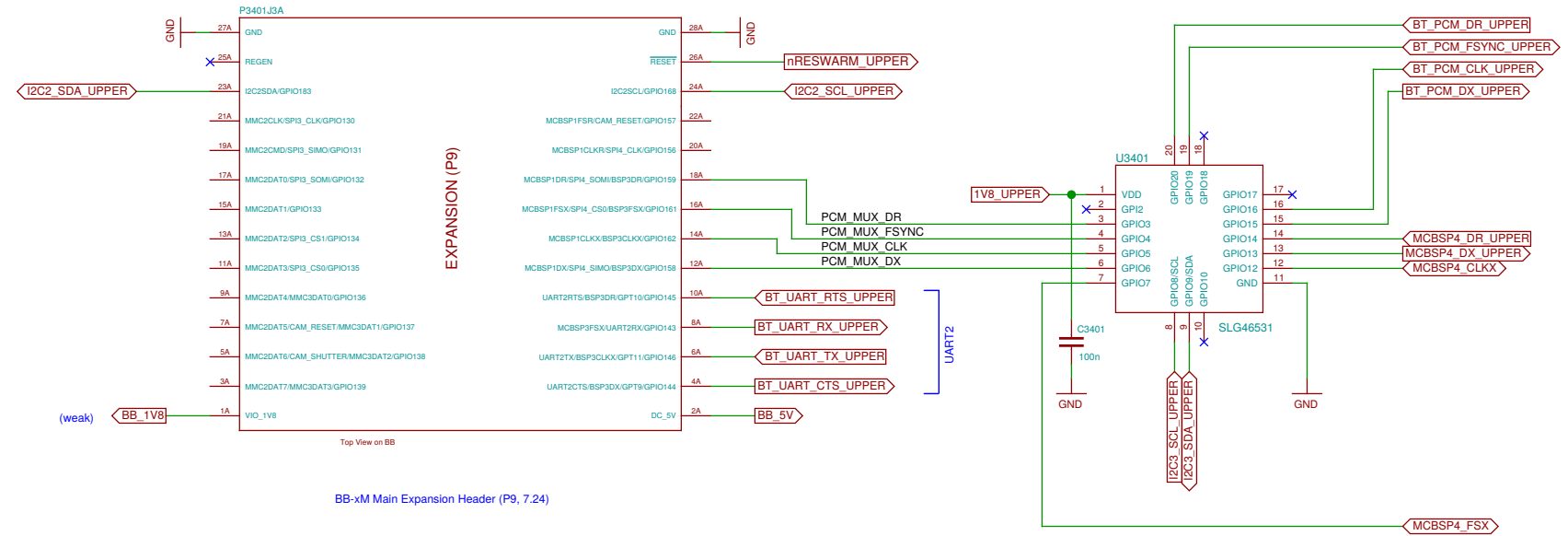


Alternative: OYKTGLJANF-0.032768

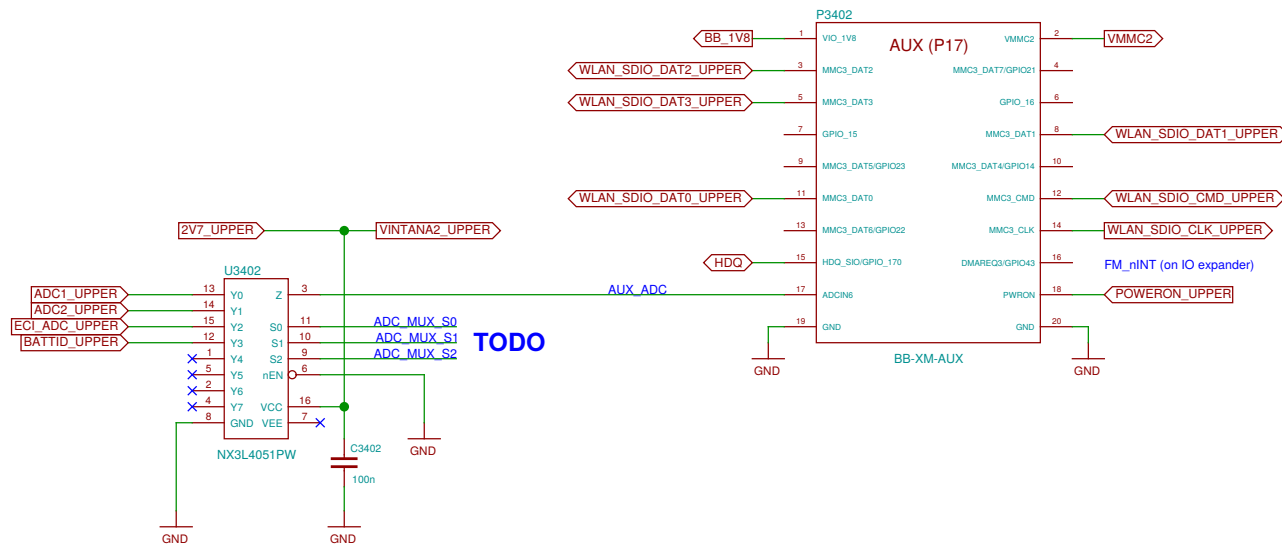
TODO: assign

- SENS_IN1
- SENS_IN2
- PENIRQ
- STYLUS_INT
- SLIDE_SW
- KEYIRQ
- RGB_INT
- RGB_CTRL_EN
- MODEM_EN_UPPER
- INA231_INT_UPPER
- NFC_INT_UPPER
- ECIO_UPPER
- ECI1_UPPER
- ECI_OUT_UPPER
- WLAN_IRQ_UPPER
- SCREEN_LOCK_UPPER
- MODEM_EMERG_UPPER
- CPU_SIM_CLK_UPPER
- CPU_SIM_IO_UPPER
- IOX1_INT_UPPER
- IOX2_INT_UPPER
- IOX3_INT_UPPER

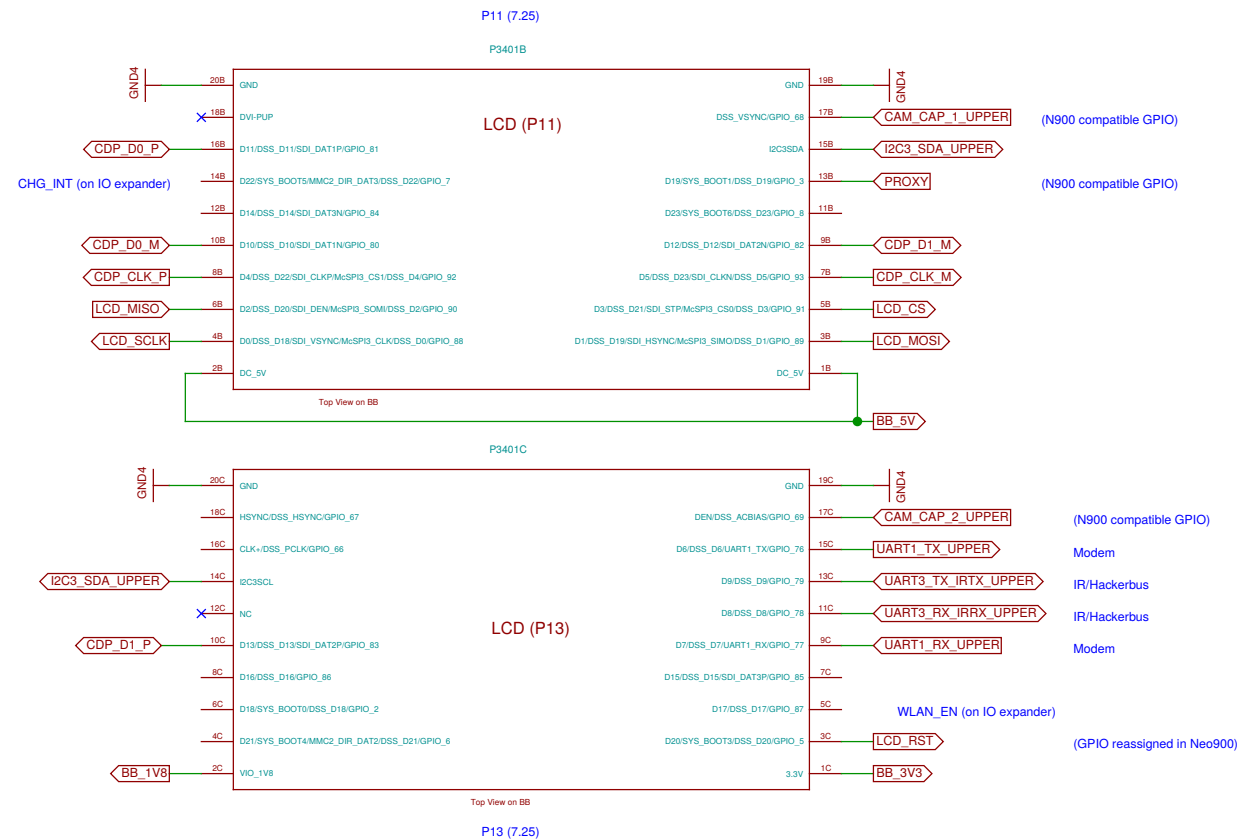
Sheet: /Connector to BB-XM/		
File: neo900_SS_33.sch		
Title: Connector to BB-XM		
Size: A3	Date: 17 JUL 2016	Rev:
Plotted by eeshow 2103115+ 20161019-02:26Z		Id: 33/37



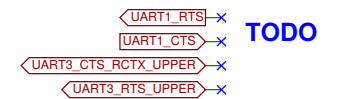
TODO: update pin names in footprint



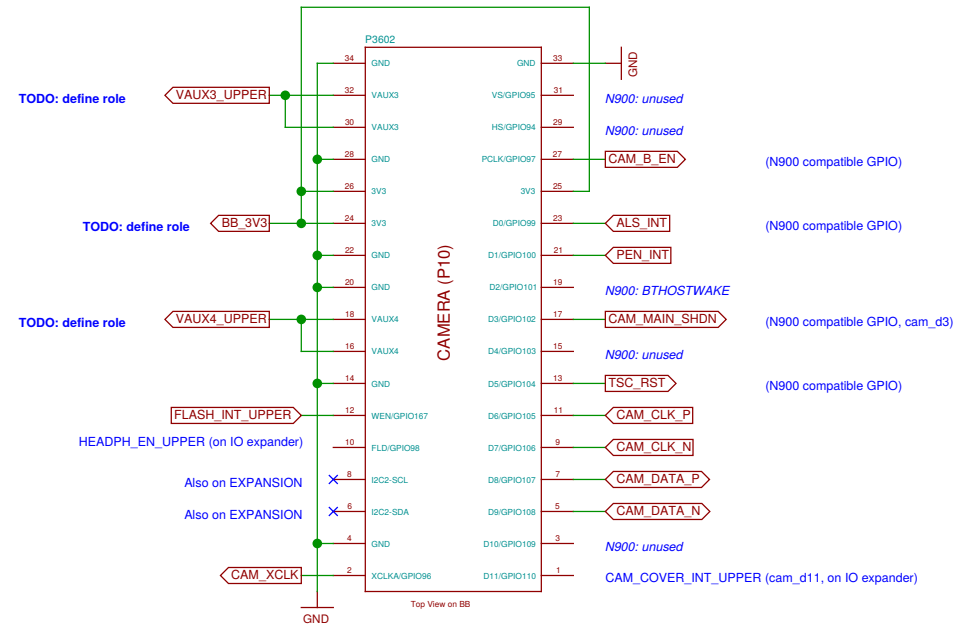
TODO



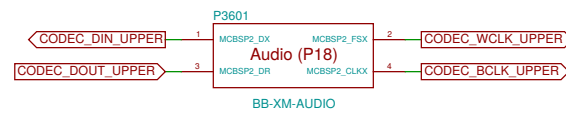
TODO: update pin names in footprint



Processor Camera Port Interface (P10, 7.20.3)



TODO: update pin names in footprint



Molex Jumper cables to connect BB-XM-Adapter to Uppwer board

N3701 15015-0439	N3702 15015-0439	N3703 15015-0439
CPU	DISP	CAM

N3704 N900 case assembly

N3705 N97-CAMERA-HOLE

N3706 headset jack

N3707 STENCIL-TOP

N3708 STENCIL-BOTTOM

Sheet: /No-Solder Components/ File: neo900_SS_37.sch		
Title: No-Solder Components		
Size: A3	Date: 17 JUL 2016	Rev:
Plotted by eeshow 2f031f5+ 20161019-02:26Z		Id: 37/37