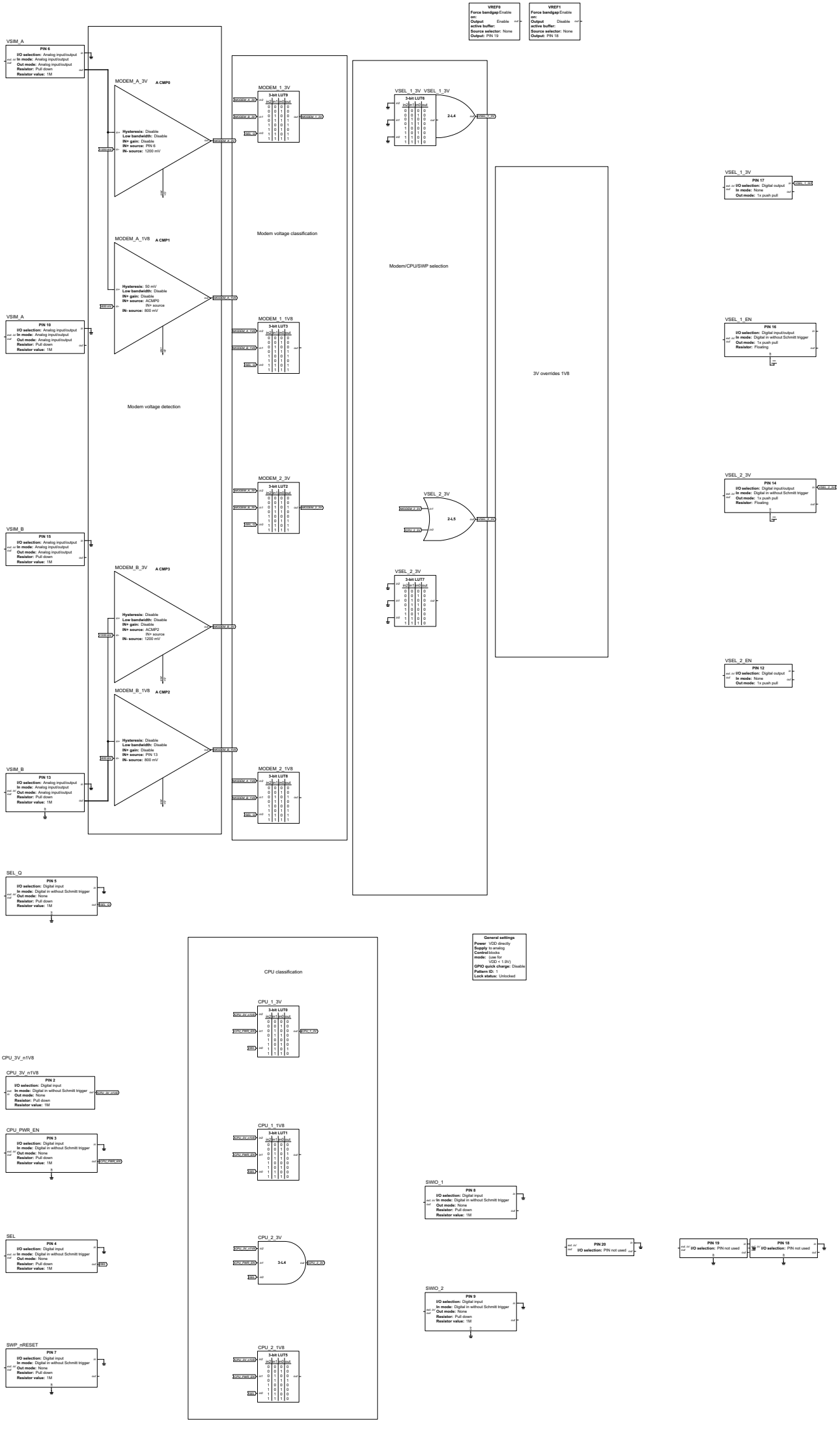
VREF0
Force bandgap on:
Enable
Output active buffer:
Enable
Source selector:
None
Output:
PIN 19
VREF1
Force bandgap on:
Enable
Output active buffer:
Enable
Source selector:
None
Output:
PIN 18
VSIM_A
PIN 6
I/O selection:
Analog input/output
In mode:
Analog input/output
Out mode:
Analog input/output
Resistor:
Pull down
Resistor value:
1M
MODEM_A_3V
A CMP0
Hysteresis:
Disable
Low bandwidth:
Disable
IN+ gain:
Disable
IN+ source:
PIN 6
IN- source:
1200 mV
MODEM_1_3V
3-bit LUT9
MODEM_A_3V
MODEM_B_3V
GND_IO
MODEM_1_3V
VSEL_1_3V
VSEL_1_3V
3-bit LUT6
2-LP4
VSEL_1_3V
Modem voltage classification
Modem/CPU/SWP selection
3V overrides 1V8
VSEL_1_3V
PIN 17
I/O selection:
Digital output
In mode:
None
Out mode:
1x push pull
VSEL_1_3V
MODEM_A_1V8
A CMP1
Hysteresis:
50 mV
Low bandwidth:
Disable
IN+ gain:
Disable
IN+ source:
ACMP0 IN+ source
IN- source:
800 mV
1800 mV
MODEM_A_1V8
VSIM_A
PIN 10
I/O selection:
Analog input/output
In mode:
Analog input/output
Out mode:
Analog input/output
Resistor:
Pull down
Resistor value:
1M
MODEM_1_1V8
3-bit LUT3
MODEM_A_1V8
MODEM_B_1V8
GND_IO
VSEL_1_EN
PIN 16
I/O selection:
Digital input/output
In mode:
Digital in without Schmitt trigger
Out mode:
1x push pull
Resistor:
Floating
Modem voltage detection
MODEM_2_3V
3-bit LUT2
MODEM_A_3V
MODEM_B_3V
GND_IO
MODEM_2_3V
VSEL_2_3V
VSEL_2_3V
2-LP5
MODEM_2_3V
GND_IO
VSEL_2_3V
PIN 14
I/O selection:
Digital input/output
In mode:
Digital in without Schmitt trigger
Out mode:
1x push pull
Resistor:
Floating
VSEL_2_3V
VSIM_B
PIN 15
I/O selection:
Analog input/output
In mode:
Analog input/output
Out mode:
Analog input/output
Resistor:
Pull down
Resistor value:
1M
MODEM_B_3V
A CMP3
Hysteresis:
Disable
Low bandwidth:
Disable
IN+ gain:
Disable
IN+ source:
ACMP2 IN+ source
IN- source:
1200 mV
1200 mV
MODEM_B_3V
MODEM_B_1V8
A CMP2
Hysteresis:
Disable
Low bandwidth:
Disable
IN+ gain:
Disable
IN+ source:
PIN 13
IN- source:
800 mV
1800 mV
MODEM_B_1V8
VSIM_B
PIN 13
I/O selection:
Analog input/output
In mode:
Analog input/output
Out mode:
Analog input/output
Resistor:
Pull down
Resistor value:
1M
MODEM_2_1V8
3-bit LUT8
MODEM_A_1V8
MODEM_B_1V8
GND_IO
VSEL_2_EN
PIN 12
I/O selection:
Digital output
In mode:
None
Out mode:
1x push pull
SEL_Q
PIN 5
I/O selection:
Digital input
In mode:
Digital in without Schmitt trigger
Out mode:
None
Resistor:
Pull down
Resistor value:
1M
SEL_IN
General settings
Power
VDD directly
Supply
to analog
Control
blocks mode:
(use for VDD < 1.9V)
GPIO quick charge:
Disable
Pattern ID:
1
Lock status:
Unlocked
CPU classification
CPU_1_3V
3-bit LUT5
CPU_3V_n1V8
CPU_PWR_EN
1800
CPU_1_3V
CPU_3V_n1V8
CPU_3V_n1V8
PIN 2
I/O selection:
Digital input
In mode:
Digital in without Schmitt trigger
Out mode:
None
Resistor:
Pull down
Resistor value:
1M
CPU_3V_n1V8
CPU_PWR_EN
PIN 3
I/O selection:
Digital input
In mode:
Digital in without Schmitt trigger
Out mode:
None
Resistor:
Pull down
Resistor value:
1M
CPU_PWR_EN
CPU_1_1V8
3-bit LUT1
CPU_3V_n1V8
CPU_PWR_EN
1800
SWIO_1
PIN 8
I/O selection:
Digital input
In mode:
Digital in without Schmitt trigger
Out mode:
None
Resistor:
Pull down
Resistor value:
1M
SEL
PIN 4
I/O selection:
Digital input
In mode:
Digital in without Schmitt trigger
Out mode:
None
Resistor:
Pull down
Resistor value:
1M
SEL
CPU_2_3V
CPU_3V_n1V8
CPU_PWR_EN
3-LP4
CPU_2_3V
1800
PIN 20
I/O selection:
PIN not used
PIN 19
I/O selection:
PIN not used
PIN 18
I/O selection:
PIN not used
SWIO_2
PIN 9
I/O selection:
Digital input
In mode:
Digital in without Schmitt trigger
Out mode:
None
Resistor:
Pull down
Resistor value:
1M
SWP_nRESET
PIN 7
I/O selection:
Digital input
In mode:
Digital in without Schmitt trigger
Out mode:
None
Resistor:
Pull down
Resistor value:
1M
CPU_2_1V8
3-bit LUT5
CPU_3V_n1V8
CPU_PWR_EN
1800